

Graduate Course for Spring 2006  
ANALOG AND LOW-POWER DIGITAL VLSI DESIGN  
16:332:577  
Section 01

Prof. Michael L. Bushnell – Rutgers University

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This course covers low-power design techniques for VLSI digital circuits, and system-on-a-chip layout integration issues between analog and digital cores. Low-power design techniques are extremely critical since chip transistor density has surpassed 220 million transistors on a chip.

We also cover transistor design and chip layout of commonly-used analog circuits such as OPAMPs, A/D and D/A converters, sample-and-hold circuits, filters, modulators, phase-locked loops, and voltage-controlled oscillators. These circuits are commonly in the front-end and back-end transceivers of mixed analog/digital *Very Large Scale Integrated Circuits* (VLSI). These circuits interface to the real world, and are therefore analog circuits. These circuits are particularly found in portable wireless systems.

The low-power digital design project can be replaced by redesign of a digital layout from the graduate course 332:574, with the goal of reducing the power consumption. The course includes two analog circuit design projects of moderate scope. Alternatively, instead of a 2nd analog design project, the student can substitute the design and completion of an analog core for a system-on-a-chip project from the course 16:332:574.

Since this is an evolving course, its content and organization will be subject to significant change over the first three years that it is taught. The course complements these existing courses in the ECE graduate curriculum:

- 332:574 Computer-Aided Digital VLSI Design
- 332:576 Testing of ULSI Circuits
- 332:555 Microwave Circuits: Design and Engineering
- 332:587 Transistor Circuit Design
- 332:588 Integrated Transistor Circuit Design
- 332:590 Integrated Circuits

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Bushnell's Office Hours: Tuesday, Thursday 3:00-6:00  
Meeting Room: Room 538, CORE Building  
Meeting Time: Friday, 6:40 p.m. – 9:30 p.m.  
First Meeting: Friday, Jan. 20, 2006  
Course Completion Date: April 28, 2006

### **TEXTS:**

1. P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. 4th Edition, New York: John Wiley and Sons, 2001, ISBN # 0-471-32168-0.
2. Kaushik Roy and Sharat C. Prasad, *Low-Power CMOS VLSI Circuit Design*. New York: John Wiley and Sons, Inc., 2000, ISBN # 0-471-11488-X.
3. Jose E. Franca and Yannis Tsividis, Editors, *Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing*, 2nd Edition, Englewood Cliffs, NJ: Prentice-Hall, Inc., 1994, ISBN # 0-13-203639-8.
4. Alan Hastings, *The Art of Analog Layout*, 1st Edition, Upper Saddle River, NJ; Prentice-Hall, Inc., 2006, 2nd edition, ISBN # 0-13-146410-8.

### **REFERENCE BOOKS:**

1. Markus Helfenstein and George S. Moschytz, Editors, *Circuits and Systems for Wireless Communications*, Boston: Kluwer Academic Publishers, 2000, ISBN # 0-7923-7722-2.
2. N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A Systems Perspective*. 2nd Edition, Reading, MA: Addison-Wesley, 1993, ISBN # 0-201-53376-6.
3. M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing: Digital, Analog, and Mixed-Signal VLSI Circuits*, Kluwer Academic Press, Boston, 2000, ISBN # 0-7923-799-1-8.
4. Shanti Pavan and Yannis Tsividis, *High Frequency Continuous Time Filters in Digital CMOS Processes*, Boston: Kluwer Academic Publishers, 2000.
5. Shahriar Rabii and Bruce A. Wooley, *The Design of Low-Voltage, Low-Power Sigma-Delta Modulators*, Boston: Kluwer Academic Publishers, 1999.
6. Emad N. Farag and Mohamed I. Elmasry, *Mixed Signal VLSI Wireless Design: Circuits and Systems*, Boston: Kluwer Academic Publishers, 1999, ISBN # 0-7923-8687-6.

7. Adam Osseiran, Editor, *Analog and Mixed-Signal Boundary-Scan: A Guide to the IEEE 1149.4 Test Standard*, Boston: Kluwer Academic Publishers, 1999, ISBN # 0-7923-8686-8.
8. Bapiraju Vinnakota, Editor, *Analog and Mixed-Signal Test*, Upper Saddle River, NJ: Prentice-Hall, Inc., 1998, ISBN # 0-13-786310-1

**ASSUMED BACKGROUND:**

Analog Electrical Network Theory	Basic Amplifier Design
Digital VLSI Design	Digital Electronics
Analog Electronics	Boolean Algebra

**WORK EXPECTED OF STUDENTS:** The course will meet once a week, for three hours, for 14 weeks. Each student will complete these items:

- 1 Digital Low-Power Layout (this can come from Digital VLSI Projects)
- 2 Moderate Analog Chip Layouts (these can come from Digital VLSI Projects)
- 1 Term Paper
- Homework

### TENTATIVE SCHEDULE OF TOPICS:

Topic	Module	Reading	Date
Introduction to Low-Power Design	1 (7)	Roy Preface, 1	1/20/06
Physics of CMOS Power Dissipation	2 (46)	Roy 2.1 - 2.3	1/20/06
Power Consumption and Limiting Factors	3 (26)	Roy 2.4	1/20/06
Introduction to Power Estimation	4 (24)	Roy 3.1 - 3.3	1/27/06
Statistical Power Estimation	5 (52)	Roy 3.4 - 3.9	1/27/06
Circuit Level Power Estimation	6 (26)	Roy 3.10 - 3.14	2/3/06
Behavioral Synthesis for Low Power	7 (42)	Roy 4.1	2/3/06
Logic/Circuit Synthesis for Low-Power	8 (37)	Roy 4.2 - 4.4	2/10/06
Design and Leakages of Low-Voltage CMOS Devices	9 (48)	Roy 5.1 - 5.8	2/10/06
Design and Test of Low-Voltage CMOS	10 (45)	Roy 5.7 - 5.9	2/17/06
Low-Power Static RAM Architectures	11 (35)	Roy 6	2/17/06
Low-Power Computing with Energy Recovery	12 (29)	Roy 7.1 - 7.2	2/24/06
Partially Reversible Logic and Quasi-Adiabatic Memories	13 (44)	Roy 7.3 - 7.5	2/24/06
Software Design for Low Power	14 (33)	Roy 8	3/3/06
Systematic Digital Low-Power Layout with Hazard Filtering and Balanced Delay	15 (1)		3/3/06
Physical Design and Layout of Passive Analog Components	16 (45)	Hastings 1 - 7	3/10/06
Diode and Transistor Theory (Review)	17 (16)		3/10/06
Physical Design and Layout of Diodes and Transistors	18 (50)	Hastings 8 - 11	3/10/06
MOS Amplifier Design	19 (72)	Gray	3/24/06
Current Source Biasing for Temperature and Supply Independence, analog OPAMP, wide-range amplifier, and analog comparator design	20 (21)	Gray 1, 3, 4, 5	3/31/06
MOS Amplifier Compensation, Miller Effect	21 (58)	Gray 6, 8, 9	4/7/06
Gilbert Cell (Analog Multiplier) Design & Layout	22 (5)	Gray 10	4/14/06
Phase-Locked Loop Layout & Voltage-Controlled Oscillator layouts	23 ()	Gray 10	4/14/06
A/D and D/A Converter Design: Successive approximation, flash, subranging, pipelined, and $\Sigma - \Delta$ layouts. Resistive Ladders & Sample-and-Hold Circuits	24 ()	Tsividis 9, 10, 11	4/14/06
Wireless Circuits	25 ()	Tsividis 12, 17	4/21/06
Filters, including Low-Pass, Band-Pass, High-Pass, Biquadratic, Leapfrog, SAW, and Switched Capacitor	26 ()	Tsividis 6, 7, 12	4/21/06
Integrated <i>Radio Frequency</i> (RF) CMOS circuit design	27 ()	Tsividis 12, 17	4/28/06

**GRADING:**

Analog Layout Design Project 1:	20%
Analog Layout Design Project 2:	20%
Digital Low-Power Layout Design Project:	20%
Term Paper:	20%
Homework:	20%
Total:	100%