

14:332:437 Digital Systems Design

Fall 2007

Problem Set 10

Electrical and Computer Engineering Department

College of Engineering

Rutgers University

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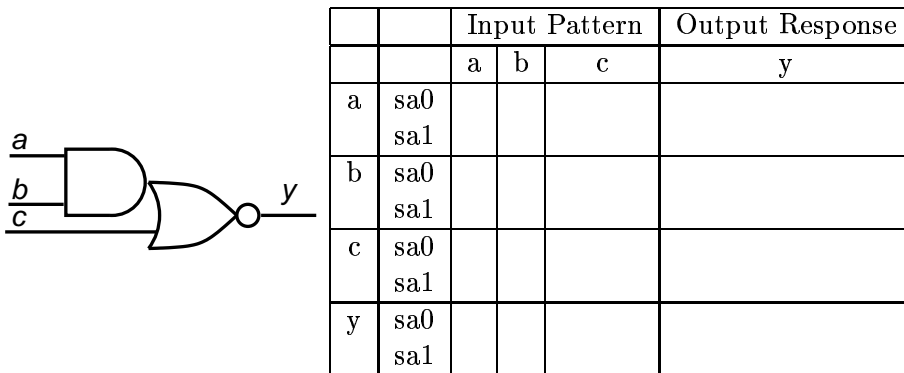
Assigned: December 5, 2007

Due: December 12, 2007

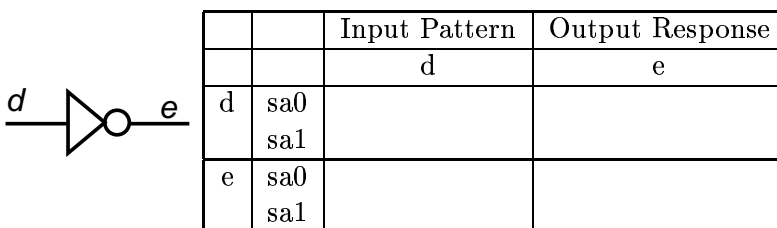
STUDENTS ARE EXPECTED TO WORK INDEPENDENTLY ON BOTH HOMEWORK AND EXAMINATIONS. NO COLLABORATION IS PERMITTED. YOUR WORK MUST BE YOUR OWN.

1. (**Test Pattern Generation.**) Calculate the test patterns for each of the three following circuits, and use the table format provided.

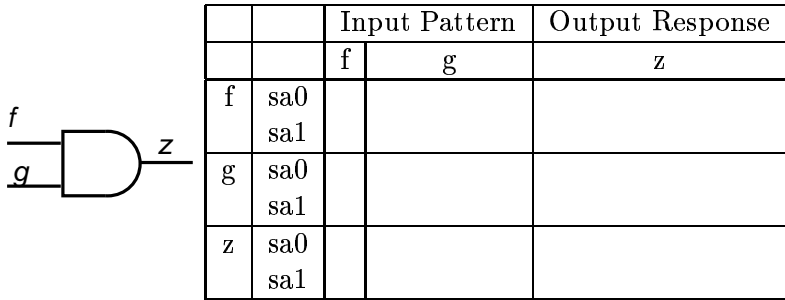
(a) First circuit:



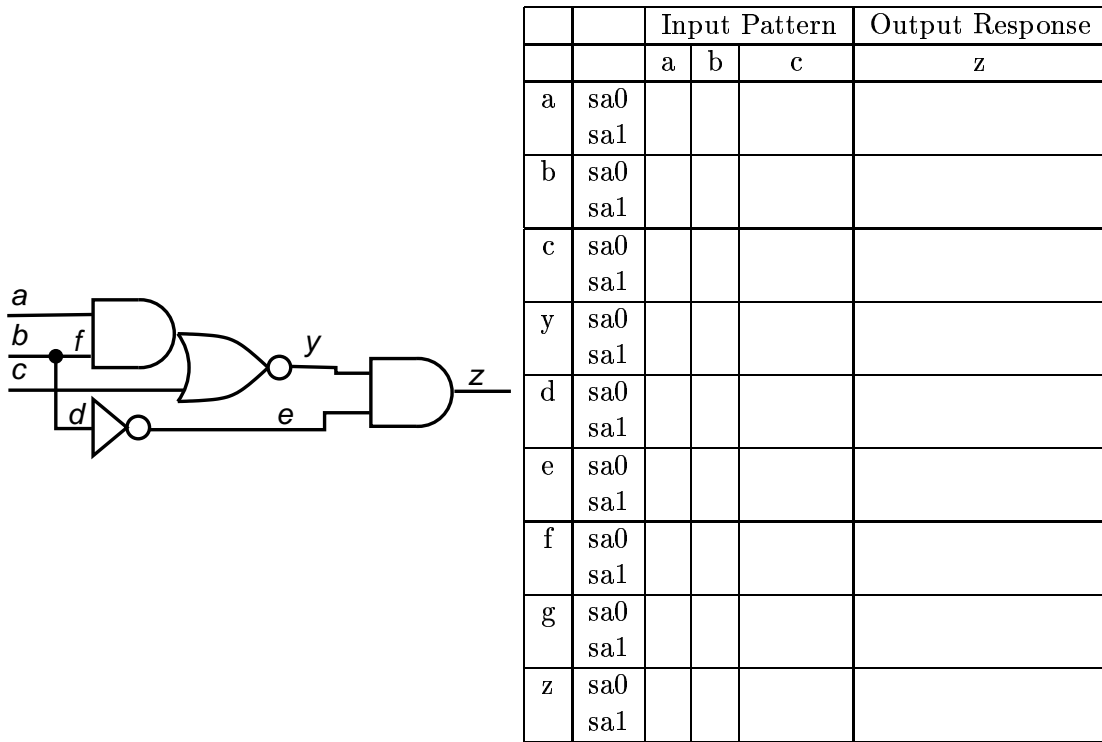
(b) Second circuit:



(c) Third circuit:



2. (**Test Pattern Generation.**) Now calculate the tests for the circuit that combines these three circuits, using the table provided. Why aren't all of the input and output faults of the three subcircuits still testable? Write an essay proposing a solution to this problem. This example illustrates why separately testable subcircuits cannot simply be combined into a more complex circuit, with their testability preserved.



3. *Built-In Self-Testing Circuits.* In the logic diagram in Figure 1, the portion of the circuit outlined in dashed lines is the actual circuit to be tested. Signals $A1$, $B1$, and $C1$ are the inputs to the circuit and signal F is the circuit output. The logic to the left of the circuit is very similar to the hardware used to calculate a cyclic code, and is called a *Linear Feedback Shift Register*. This register is initialized to $Q1 Q2 Q3 = "001"$ for normal circuit operation, and Inputs A , B and C are then used to drive signals $A1$, $B1$ and $C1$ in functional operation mode when $TEST = 0$. The circuit output is taken from signal F . The logic to the right of the circuit output F is also very similar to the cyclic code generator, and is called a *Signature Analysis Register*. The Signature Analysis Register is not used in normal circuit operation, and outputs $S1$, $S2$ and $S3$ are ignored during normal operation.

In test mode, the normal inputs A , B and C are ignored, and $TEST = 1$. We initialize all flip-flops by setting signal \overline{RESET} to 0 and then restoring it to 1. This initializes $Q1 Q2 Q3$ to “001” and $S1 S2 S3$ to “000”. We then clock the circuit for 7 clock periods on the clock lines CL . The Linear Feedback Shift Register will generate the input sequence $001 \rightarrow 100 \rightarrow 010 \rightarrow 101 \rightarrow 110 \rightarrow 111 \rightarrow 011 \rightarrow 001$. During the seven clock periods while we are generating this sequence, the *Signature Analysis Register* is also clocked, and will compute a polynomial division remainder very like the cyclic codes discussed in the course. After the seven clock periods, signals $S1 S2 S3$ will contain a three-bit number known as the *signature* of the circuit. If the circuit has no signal lines permanently stuck-at 0 or 1, this signature will be the signature of the *good machine*. When we manufacture this circuit in volume, we will repeat this testing sequence for each copy of the circuit, and examine $S1 S2 S3$ after testing. If a manufactured circuit generates the good machine signature, then it is assumed to be correct. Circuits that generate incorrect (*failing machine*) signatures are rejected.

For this problem:

- (a) Describe the entire circuit, including the test hardware, in **structural** Verilog. Turn in Verilog code, a system block diagram (from Synopsys), and a logic schematic generated by the Synopsys system.
- (b) Simulate the circuit in normal operation mode (initialize all flip-flops to ‘0’ and hold $CL = 0$). Verify that the circuit works correctly for all eight input combinations of $A B C$.
- (c) Operate the circuit in test mode, under the conditions described above, but with $TEST = 1$ and CL pulsing. Use **vcs** to calculate the final values of $S1 S2 S3$ for the *good machine signature*.
- (d) Cause **vcs** to model the single fault f stuck-at 0 by permanently connecting f to logic ‘0’. Calculate the *failing machine signatures* for this circuit fault.
- (e) Again use **vcs** to calculate the failing machine signature for single signal e stuck-at 1.
- (f) Explain which of the above faults are detected and why are they detected.
- (g) Compute the machine signature (using **vcs**) for the multiple fault case of signal f stuck-at 1 and signal e stuck-at 0 simultaneously.
- (h) What should be done to this circuit to improve the probability that any faulty logic signal in the circuit will be detected?

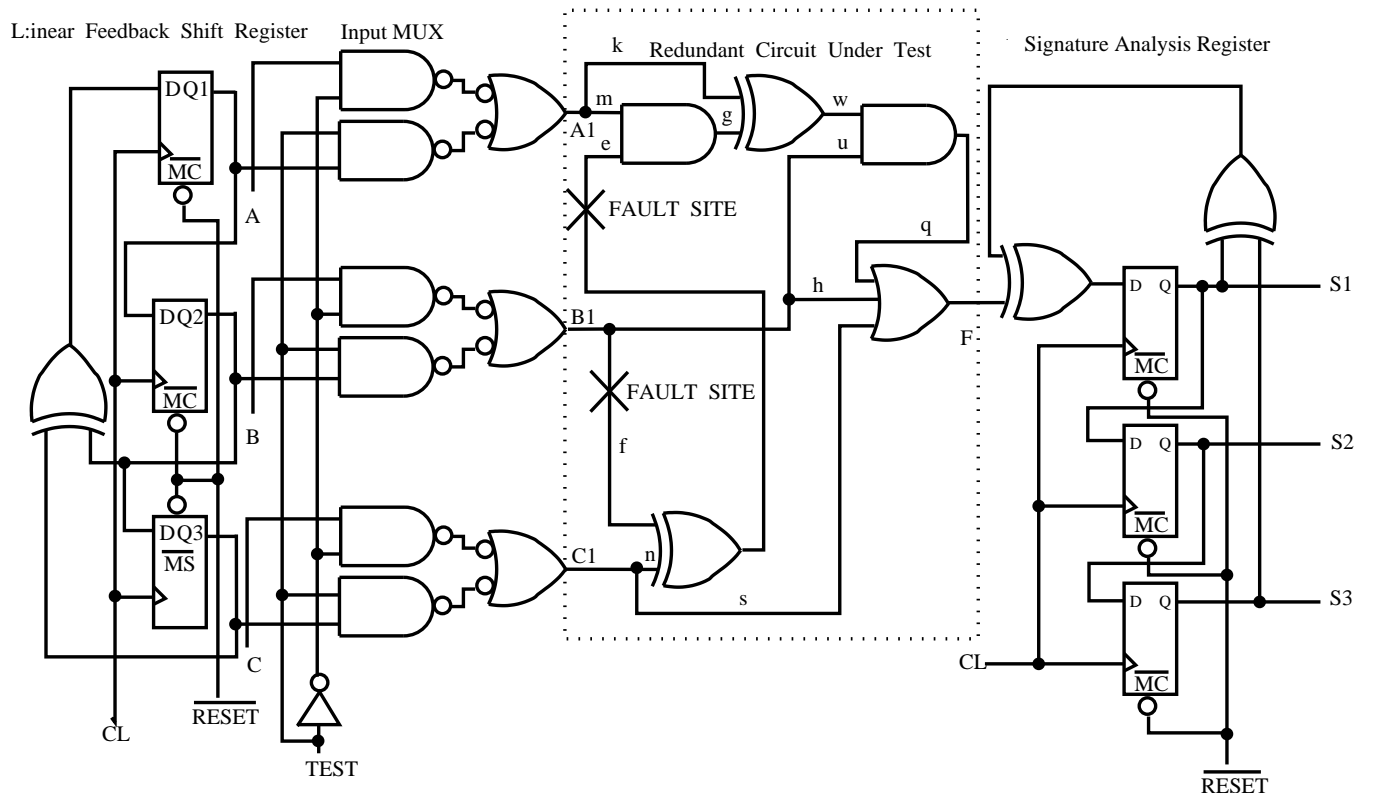


Figure 1: Hardware for Problem 1