

14:332:437 Concepts in Digital Systems Design
Fall 2009
Problem Set 1
Electrical and Computer Engineering Department
College of Engineering
Rutgers University

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Assigned: September 9, 2009

Due: September 23, 2009

STUDENTS ARE EXPECTED TO WORK INDEPENDENTLY ON BOTH HOMEWORK AND EXAMINATIONS. NO COLLABORATION IS PERMITTED. YOUR WORK MUST BE YOUR OWN.

1. Complete the ordinary Karnaugh map to realize the function $G(a, b, c, d, e, f)$ given by the truth table in Table 1. Create a six-variable ordinary Karnaugh map for G . Write the canonical **Standard Minimal Product-of-Sums Form** for G . Draw the minimal logic gate realization of G using only NOR gates and INVERTERS. No credit will be given for circuits with prohibited gate types, work missing a Karnaugh map, or work that does not give a Product-of-Sums form.
2. Implement the following function $G(a, b, c, d, e, f, h, k, m, n, p, r, s, t, u, w, y, z)$ given in the truth table given in Table 2 using an *indirect-addressed* MUX. Simplify the Boolean expressions in the truth table and put them into equivalent form. Use a, b, c, d, e as *Control Variables* and $f, h, k, m, n, p, r, s, t, u, w, y, z$ as *Map-entered Variables*. You may use only an *8-input, 1-output* MUX and a ROM to implement this in hardware. Your ROM addresses should be selected by a, b, c, d, e in that order. No credit will be given if you do not use an *8-input, 1-output MUX*, if you do not use a ROM, or if your map entered and control variables violate the specifications.

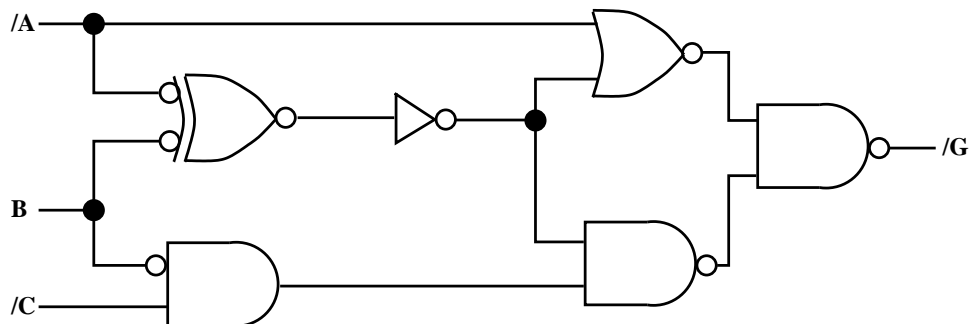
Table 1: Truth Table for Problem 1

e	f	a	b	c	d	G	e	f	a	b	c	d	G
0	0	0	0	0	0	1	1	0	0	0	0	0	1
0	0	0	0	0	1	0	1	0	0	0	0	1	0
0	0	0	0	1	0	1	1	0	0	0	1	0	0
0	0	0	0	1	1	X	1	0	0	0	1	1	1
0	0	0	1	0	0	0	1	0	0	1	0	0	X
0	0	0	1	0	1	1	1	0	0	1	0	1	1
0	0	0	1	1	0	0	1	0	0	1	1	0	1
0	0	0	1	1	1	1	1	0	0	1	1	1	X
0	0	1	0	0	0	0	1	0	1	0	0	0	1
0	0	1	0	0	1	1	1	0	1	0	0	1	1
0	0	1	0	1	0	0	1	0	1	0	1	0	1
0	0	1	0	1	1	0	1	0	1	0	1	1	0
0	0	1	1	0	0	1	1	0	1	1	0	0	X
0	0	1	1	0	1	0	1	0	1	1	0	1	X
0	0	1	1	1	0	0	1	0	1	1	1	0	X
0	0	1	1	1	1	0	1	0	1	1	1	1	X
0	1	0	0	0	0	1	1	1	0	0	0	0	0
0	1	0	0	0	1	0	1	1	0	0	0	1	1
0	1	0	0	1	0	0	1	1	0	0	1	0	X
0	1	0	0	1	1	X	1	1	0	0	1	1	0
0	1	0	1	0	0	0	1	1	0	1	0	0	1
0	1	0	1	0	1	1	1	1	0	1	0	1	1
0	1	0	1	1	0	X	1	1	0	1	1	0	0
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	0	0	1	1	1	1	0	0	0	1
0	1	1	0	0	1	1	1	1	1	0	0	1	1
0	1	1	0	1	0	0	1	1	1	0	1	0	1
0	1	1	0	1	1	0	1	1	1	0	1	1	1
0	1	1	1	0	0	1	1	1	1	1	0	0	1
0	1	1	1	0	1	0	1	1	1	1	0	1	0
0	1	1	1	1	0	0	1	1	1	1	1	0	1
0	1	1	1	1	1	0	1	1	1	1	1	1	X

Table 2: Truth Table for Problem 2

a	b	c	d	e	G
0	0	0	0	X	$h \bar{k}$
0	0	0	1	0	$\overline{p r}$
0	0	0	1	1	$k \oplus \overline{m}$
0	0	1	0	0	$\overline{s + t}$
0	0	1	0	1	$\overline{\overline{m} + \overline{n}}$
0	0	1	1	X	$\overline{k \oplus m}$
0	1	0	0	0	$\overline{p} + \overline{r}$
0	1	0	0	1	$f + f k$
0	1	0	1	X	$y \overline{y}$
0	1	1	X	X	$f + f \overline{m}$
1	0	0	0	0	$z + \overline{z}$
1	0	0	0	1	$\overline{s} \overline{t}$
1	0	0	1	0	$k \oplus m$
1	0	0	1	1	$m n$
1	0	1	0	0	$m n + m n r$
1	0	1	0	1	$\overline{k \oplus \overline{m}}$
1	0	1	1	X	f
1	1	0	X	X	$k \oplus m$
1	1	1	X	X	$\overline{\overline{h} + k}$

3. Convert the following circuit schematic into **MIXED** logic notation. You must not change the circuit logic function nor the variable labels, but you can substitute equivalent logic gates for the ones in the circuit. Your mixed-logic notation circuit should have wires only with bubbles at both ends, or with no bubbles at either end. If an input (output) is specified as active-low, then its wire must only go to logic gates with bubbles at the corresponding input.



4. You are to design an autopilot for the wing flap controls for the new Boeing Dreamliner commercial jet airplane. All three control sub-systems for the auto-pilot are digital and have identical functionality, so you can use triple modular redundancy. Use 3 digital triple modular redundancy voters to vote on the outputs of the 3 identical systems, to produce 3 voted outputs. Please also put D flip-flops on your voters. Then, convert the voted outputs to analog signals with a D/A converter. Use flux-summing as the voting mechanism on the 3

analog outputs to send a single signal to the flap control motor. Each of the three sub-systems performs self-diagnostics to allow faults to be detected. If a fault is detected, the affected sub-system will remove itself from the flux-summing arrangement, and it is replaced by a fourth single hot standby sub-system. Assume that each sub-system has an set of eight digital inputs $I (0 .. 7)$, 8 digital inputs *Feedback* ($0 .. 7$) coming from the flap position sensor, and eight digital outputs *Command* ($0 .. 7$), which are its digital command to the flap control motor. The 3 voted digital outputs must be converted into 3 analog signals, using D/A converters, before the flux summer can vote on them. Each sub-system also has an output signal *Broken*, which is logic 1 when the checker indicates that the sub-system's output differs from the voted output. Please design a flux summer for this system and bus multiplexers to replace a broken sub-system with the standby sub-system. Your hardware should also set an output warning signal *Compromised* to logic 1 when two or more sub-systems indicate that they are broken. Also include the logic schematics for the voter and for the system checker. Airbus jets and certain Boeing jet rudder controls have been implicated in fatal crashes where either a control unit failed, or the control unit jammed because the pilot tried to change the settings too fast.