

Course Syllabus  
14:332:438 Capstone Design – Computer Systems, DSD Track  
Section 1  
Spring 2009  
Electrical and Computer Engineering Department  
School of Engineering  
Rutgers University

Prof. Michael L. Bushnell

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**PHILOSOPHY:** This is the design companion course to 14:332:437 *Concepts in Digital Systems Design*. This is exclusively a project design course, and your entire grade is determined by your group project. You will apply the concepts you learned in 332:437 in order to design a large hardware system in this course, and prototype it on field-programmable gate arrays. The entire class will be organized into 5 or 6-person design teams, each of which will complete a significant project by the end of the term. Part of your course grade is determined by the success of your project team, and the rest of your grade is determined by the quality of your own design effort.

**COURSE DESCRIPTION:** The first week of this course will be spent organizing the class into design teams, and then a weekly 15-minute meeting will be arranged for each team. There will be a few lectures on FPGA technology, and three meetings at the end of the course for final project presentations.

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Course Laboratory:	EE 103 UNIX Work Station Room
Course Web site:	<a href="http://www.caip.rutgers.edu/~bushnell">http://www.caip.rutgers.edu/~bushnell</a>
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**PREREQUISITES:**

- 332:231 Digital Logic Design
- 332:233 Digital Logic Design Lab.
- 332:331 Computer Architecture and Assembly Language
- 332:333 Computer Architecture Lab.
- 332:437 Digital Systems Design

**TWO-TERM SEQUENCE:** This required course is the second part of a two-term sequence. This course is a pure design course, with little academic content, and the combination of the 332:437 and 332:438 courses satisfies the ECE Dept. capstone design course requirement.

**TEXTS:**

- *Self-Checking and Fault-Tolerant Digital Design*, by Lala, Academic Press/HBJ, ISBN # 0-12-434370-8.
- *The Verilog Hardware Description Language*, by Don Thomas and Philip Moorby, Kluwer Academic Publishers, 5th Edition, 2003, ISBN # 1-4020-7089-6.
- Optional Text: *Logic Design & Switching Theory*, by Muroga, Krieger Publishing Co., ISBN # 1-57524-036-X.
- Optional Text: *Digital Design Principles and Practices*, by John F. Wakerley, Prentice Hall.

**COMPUTER USAGE:** Students will use the Synopsys logic synthesis system to design and simulate hardware described in the VERILOG hardware description language, in order to stage the hardware system that you have designed on a Field-Programmable Gate Array.

<b>GRADING:</b>	Overall Course Project Quality	50 %
	Your Personal Effort on the Project	50 %

**POLICIES:**

1. Constructive suggestions from students about this course will be greatly appreciated.
2. STUDENTS ARE EXPECTED TO COLLABORATE ON THE PROJECT, WHICH MUST BE A GROUP EFFORT of AT LEAST 5 or 6 STUDENTS.
3. The schedule below indicates when each component of the project is due. The penalty for missing a due date is that you lose 1/2 of a letter grade in this course. The only exceptions will be in the case of illness, death in the family, extraordinary family circumstances, or computer failure at Rutgers.
4. All course materials are available on the course web site:  
<http://www.caip.rutgers.edu/~bushnell>
5. Do your lab work early – this will give you a chance to get on the computer. Most students let lab work wait until the night before it is due, and then are unable to get a computer because they are all taken.

## ASSUMED BACKGROUND

- Boolean Algebra
- Combinational and Sequential Circuit Logic Design
- All kinds of flip-flops and latches
- Electrical Network Theory
- C and/or C++ Language Programming
- RISC Computer Architecture
- VERILOG Hardware Description Language

If you are unfamiliar with any of these concepts, you should immediately drop this course.

## COURSE MEETING OUTLINE

#	Description	Date
1	PROJECT TEAM ORGANIZATION	1/23/09
2-8	WEEKLY PROJECT TEAM MEETINGS	1/30/09 – 3/13/09
9	FIELD PROGRAMMABLE GATE ARRAY LECTURE (FPGAs)	3/27/09
10	FPGA DOWNLOADING LABORATORY (ALL GROUPS)	4/3/09
11-13	WEEKLY PROJECT TEAM MEETINGS	4/10/09 – 4/24/09
14	FINAL PROJECT PRESENTATIONS (ALL GROUPS)	5/1/09

## PROJECT SCHEDULE

Date	Required Activity Description	Late Penalty	Grade Effect
1/30/09	Project Proposals with Work Assignment Due	- 1/2 Course Grade	A
2/6/09	Project Specification & System Block Diagram Due	- 1/2 Course Grade	A–
2/13/09	System Timing Diagram Due	- 1/2 Course Grade	B+
2/13/09	Economic and Cost Analysis of Project Due	- 1/2 Course Grade	B
2/27/09	Behavioral VERILOG Code Review	- 1/2 Course Grade	B–
3/27/09	Behavioral VERILOG Code Due	- 1/2 Course Grade	C+
3/27/09	Behavioral VERILOG Simulation Due	- 1/2 Course Grade	C
4/10/09	Testing Method Hardware Due	- 1/2 Course Grade	C–
4/10/09	Synthesized VERILOG Logic Due	- 1/2 Course Grade	D+
4/10/09	Logic VERILOG Simulation Due	- 1/2 Course Grade	D
4/10/09	Project Safety and Environmental Impact Statement Due	- 1/2 Course Grade	D–
4/10/09	Revised project Cost Figures Due	- 1/2 Course Grade	F+
4/24/09	Testing Fault Coverage and Test Patterns Due	- 1/2 Course Grade	F
5/1/09	Final Project Presentation Due	- 1/2 Course Grade	F–
5/1/09	FPGA Fitted Hardware Realization Due	- 1/2 Course Grade	F– –
5/1/09	Final Project Report Due	- 1/2 Course Grade	F– – –

Your final projects will be graded on the following criteria:

- The presence of a clear Data Book Description.
- Quality of the Project Specifications.
- Logical correctness (shift registers that don't shift will cost you points).
- Speed and throughput (hardware that cannot achieve your specified clock rate will cost you points).
- Correct use of logic circuit simulation and FPGA tools.
- Quality of the documentation (if it is a mess, you will lose points).
- Presence of a Cost Analysis for this Design.
- Presence of Environmental Impact and Health and Safety Description for this Design (where appropriate).

Verify logical correctness as you progress in the design phase, not after the whole thing is completed.

## PROJECT IDEAS

Below are some project ideas. You need not choose a project from this list. It is not necessary that your project be a brand new innovation. However, I strongly encourage you to be creative. I will not accept any digital alarm clock or parallel multiplier designs. This course presents an exciting design opportunity, and each group must come up with its own project proposal! I hope that your project will reflect some of the things I have been stressing in this course sequence, such as regularity, logical correctness, fault-tolerance, testing, high-speed arithmetic, etc.

1. Design a 32-bit microprocessor.
2. Design a 16-bit Digital Signal Processor.
3. Design a hierarchical memory system, with high-speed cache, DRAM, and flash DRAM implemented as a multi-level, virtual memory system.
4. Design a high-speed floating point arithmetic processor like the Wytex chips.
5. Design a programmable I/O controller.
6. Design an image processing hardware system that can do the Hough transform, the Discrete Cosine Transform, and all of the frequently-used transforms for image processing.
7. Design an advanced home automation and security system.
8. Design a map and trip routing system for an automobile.
9. Design a knock-out switch for an *Asynchronous Transfer Mode* (ATM) internet switch.
10. Design a baseband processor and a microprocessor for one of the communication system protocols of our time: GPS, 802.11, 802.16, Bluetooth, CDMA Cellular Telephone, etc.
11. Design an MPEG player.
12. Design a Personal Data Assistant.

13. Design an elevator controller for a bank of 10 elevators spanning 30 floors in the Empire State Building.

These are only suggestions, but represent some of the better hardware designs that have been done at Carnegie Mellon, Duke, and Rutgers.

#### REFERENCE BOOKS:

- VERILOG Books:

- *Verilog HDL*, by Samir Palnitkar, Prentice Hall, 2003, ISBN # 0-13-044911-3.
- *Advanced Digital Design with the Verilog HDL*, by Michael D. Ciletti, Prentice Hall, 2003, ISBN # 0-13-089161-4.

- Fault Tolerance and Testing:

- *Design and Analysis of Fault Tolerant Digital Systems*, by Barry W. Johnson, Addison Wesley (out of print). A great tutorial book on fault tolerance and testing.

- Architecture:

- *Structured Computer Organization*, by Andrew S. Tanenbaum, Prentice Hall, 1990.

- Finite State Machines:

- *Switching and Finite Automata Theory*, by Kohavi, McGraw-Hill, 1978. THE classic book on finite state machines.

- Programmable Logic:

- *Digital Systems Design with Programmable Logic*, by Martin Bolton, Addison Wesley, 1990. A very well-written book that is, unfortunately, quite out of date because it does not mention field-programmable gate arrays.

- Digital Logic Design:

- *Digital Design – Principles and Practices*, 2nd Edition, by John F. Wakerly, Prentice-Hall, 1994. A good introduction to logic design.
- *Modern Digital Systems Design*, by John Cheung and Jon Brederson, West Publishing Co.

- Digital Circuit Testing:

- *Essentials of Electronic Testing: Digital, Analog, and Mixed-Signal*, Bushnell and Agrawal, Kluwer Academic Press, Boston, 2000, third printing, ISBN # 0-7923-799-1-8.