

Curriculum Vitae

ELECTRICAL ENGINEER and COMPUTER ENGINEER

Tenured Full Professor

United States Citizen

Age 55

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Michael Lee Bushnell

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Research Interests – Computer Engineering

Computer Aided Design (CAD) of Very Large Scale Integrated (VLSI) Circuits.

Computer algorithms for functional and structural *automatic test-pattern generation* (ATPG) for stuck-faults and path delay-faults in extremely large sequential circuits, including systems-on-a-chip. ATPG algorithms for testing mixed analog/digital circuits, where the digital part is a *digital signal processing* (DSP) circuit and the analog part contains A/D and D/A converters, filters, and mixers. *Design for circuit testability* methods and *built-in self-testing* (BIST) circuits for testing stuck-faults, delay-faults, and analog faults in large sequential circuits. Methods for finding false timing paths in combinational and sequential circuits. Global optimization algorithms for *automatic logic resynthesis* to remove false timing paths. Low-power design of VLSI circuits. Formal hardware verification of finite state machines. Nanotechnology. Design of wireless baseband processors for portable electronics, including cognitive radio applications and medical applications.

Awards and Honors

1. Nomination of the paper “A Novel Dynamic Power Cutoff Technique (DPCT) for Active Leakage Reduction in Deep Submicron CMOS Circuits,” for a *Best Paper Award, The Int’l. Symp. on Low-Power Electronics and Design, 2006*.
2. *N. N. Biswas Best Student Paper Prize*, “An Area Efficient Mixed-Signal Test Architecture for Systems-on-a-Chip,” *19th Int’l. Conference on VLSI Design (VLSI Design 2006)*, Jan., 2006, Hyderabad, India, H. Venkatanarayanan* and M. L. Bushnell.
3. Technical Program Committee Co-Chairman, *19th Int’l. Conference on VLSI Design (VLSI Design 2006)*, Jan., 2006, Hyderabad, India.
4. *Best Student Paper Prize*, “New Graphical I_{DDQ} Signatures Reduce Defect Level and Yield Loss,” *North Atlantic Test Workshop*, May, 2002, L. Rao*, M. L. Bushnell, and V. D. Agrawal.
5. Helped his students, Ganapathy Parthasarathy* and Madhu Iyer*, design the Prize VLSI Chip *A Branch Prediction Controller for a RISC Processor* that uses Built-In Self-Test and Boundary Scan. This was judged the best novice chip design in the United States in the 1996 Mentor Graphics National Chip Design competition – \$ 5000.
6. *Honorable Mention Award* for the paper “Test Generation for Mixed-Signal Devices Using Signal Flow Graphs,” *The 9th Int’l. Conference on VLSI Design (VLSI Design ’96)*, 2000 Rupees.

Fall, 2005	332:437 Concepts in Digital Systems Design	3	2 hr. 40 min.
	332:479 Concepts in VLSI Design	3	2 hr. 40 min.
	332:574 CAD Digital VLSI Design	3	2 hr. 40 min.
Spring, 2005	332:438 Capstone Design – Digital Systems	3	2 hr. 40 min.
	332:480 Capstone Design – VLSI Design	3	2 hr. 40 min.
	332:578 Deep Submicron VLSI Design	3	2 hr. 40 min.
Fall, 2004	332:437 Concepts in Digital Systems Design	3	2 hr. 40 min.
	332:479 Concepts in VLSI Design	3	2 hr. 40 min.
	332:574 CAD Digital VLSI Design	3	2 hr. 40 min.
Spring, 2004:	332:576 Testing of ULSI Circuits	3	2 hr. 40 min.
	332:574 CAD Digital VLSI Design	3	2 hr. 40 min.
Fall, 2003:	Sabbatical at the ECE Dept., U. of Canterbury, Christchurch, New Zealand		
Spring, 2003:	332:577 Analog and Low-Power Digital VLSI Design	3	2 hr. 40 min.
	332:576 Testing of ULSI Circuits	3	2 hr. 40 min.
Fall, 2002:	332:473 Introduction to VLSI Design	4	2 hr. 40 min.
	332:574 CAD Digital VLSI Design	3	2 hr. 40 min.
Spring, 2002:	332:577 Analog and Low-Power Digital VLSI Design	3	2 hr. 40 min.
	332:576 Testing of ULSI Circuits	3	2 hr. 40 min.
Fall, 2001:	332:473 Introduction to VLSI Design	4	2 hr. 40 min.
	332:574 CAD Digital VLSI Design	3	2 hr. 40 min.
Spring, 2001:	332:577 Analog and Low-Power Digital VLSI Design	3	2 hr. 40 min.
	332:576 Testing of ULSI Circuits	3	2 hr. 40 min.
Fall, 2000:	332:473 Introduction to VLSI Design	4	2 hr. 40 min.
	332:574 CAD Digital VLSI Design	3	2 hr. 40 min.
Spring, 2000:	332:576 Testing of ULSI Circuits	3	2 hr. 40 min.
Fall, 1999:	332:473 Introduction to VLSI Design	4	2 hr. 40 min.
	332:574 CAD Digital VLSI Design	3	2 hr. 40 min.
	332:431 Digital Systems Design	3	2 hr. 40 min.
Spring, 1999:	332:576 Testing of ULSI Circuits	3	2 hr. 40 min.
Fall, 1998:	332:473 Introduction to VLSI Design	4	2 hr. 40 min.
	332:574 CAD Digital VLSI Design	3	2 hr. 40 min.
	332:431 Digital Systems Design	3	2 hr. 40 min.
Spring, 1998:	332:576 Testing of ULSI Circuits	3	2 hr. 40 min.
Fall, 1997:	332:473 Introduction to VLSI Design	4	2 hr. 40 min.
	332:574 CAD Digital VLSI Design	3	2 hr. 40 min.
	332:431 Digital Systems Design	3	2 hr. 40 min.
Spring, 1997:	332:366 Digital Electronics	3	2 hr. 40 min.
	332:368 Digital Electronics Laboratory	1	1 hr. 30 min.
	332:576 Testing of ULSI Circuits	3	2 hr. 40 min.
Fall, 1996:	332:473 Introduction to VLSI Design	4	2 hr. 40 min.
	332:574 CAD Digital VLSI Design	3	2 hr. 40 min.

Sept. 1979 - Aug. 1981.

Applicon, Inc. (now Schlumberger, Ltd.). CAD/CAM Systems Manufacturer.

Advanced System Development Department – new product development.

Position: Member of Technical Staff – supervised a Mathematician.

- Wrote initial specifications for the *Applicon Graphics Language* (AGL), a PL/1-based geometric programming language. Implemented the run-time system, the code generator, and the listing module for the AGL language preprocessor.

June 1976 - Sept. 1979.

Instron Corporation, Canton, Mass. Manufacturer of instruments and laboratory computer systems. Computer Systems Department.

Position: Senior Systems Programmer – supervised two programmers.

- Founded Instron’s computerized instrumentation product line, along with six others. Defined the scope of the product and selected hardware and software components. Wrote a high-level, real-time software driver to interface Instron’s entire line of mechanical testing instruments to the DEC PDP-11 executive (RSX11M), and to the FORTRAN and BASIC compilers.
- Completed the first digital computer data-acquisition and control system for thermal-mechanical fatigue testing of jet engine turbine blades at Pratt and Whitney Aircraft. The system provided more accurate turbine blade failure data than existing systems.

July 1974 - June 1976.

Honeywell Information Systems, Computer Engineering Operations, Billerica Mass.

Computer manufacturer. Design Automation Department.

Position: Associate Engineer

- Redesigned and extended a firmware compiler for the hardware description language, RTL.

Publications

Books: (Graduate Students supervised indicated by *, Undergraduate Students by **)

1. *Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits*, Kluwer Academic Publishers, Boston, 690 p., Nov. 10, 2000, M. L. Bushnell and V. D. Agrawal, in 3rd printing. In use at the Oregon Graduate Center, Carnegie Mellon U., the U. of Wisconsin, the U. of Illinois, the Indian Institute of Technology, Bombay, the Indian Institute of Technology, Madras, Rutgers U., the U. of Michigan, the U. of Massachusetts, Amherst, Bristol U., Duke U., Tufts U., Case Western Reserve U., Nara Institute of Science and Technology (Japan), the U. of Washington, Seattle, the U. of Texas at Dallas, the U. of Bologna (Italy), McMaster U. (Canada), U. of Kuwait, U. of Rochester, U. of Southampton (U. K.), China U. of Hong Kong, and Northeastern U.
2. *Efficient Branch and Bound Search with Application to Computer Aided Design*, Kluwer Academic Publishers, Boston, 160 p., Dec. 1995, X. Chen*, and M. L. Bushnell
3. *Neural Models and Algorithms for Digital Testing*, Kluwer Academic Publishers, Boston, 208 p., June 1991, S. T. Chakradhar*, V. D. Agrawal, and M. L. Bushnell
4. *Design Automation*, Academic Press, 481 p., May, 1988, M. L. Bushnell

Refereed Journal Articles:

(Graduate Students supervised indicated by *, Undergraduate Students by **)

1. “Transistor Sizing of Logic Gates to Maximize Input Delay Variability,” *JOLPE – J. of Low Power Electronics*, accepted, 2006, T. Raja*, V. D. Agrawal, and M. L. Bushnell.

2. "A Complete Characterization of Path Delay Faults Through Stuck-At Faults," *J. of Computer and Information Sciences*, vol. 35, no. 7, July, 2003, pp, S. Majumder*, B. Bhat-tacharya, V. D. Agrawal, and M. L. Bushnell.
3. "Improving Path Delay Testability of Sequential Circuits," *IEEE Trans. on VLSI Systems*, vol. 8, no. 6, Dec. 2000, pp 736-741, T. J. Chakraborty*, V. D. Agrawal, and M. L. Bushnell.
4. "False-Path Removal Using Delay Fault Simulation," *Journal of Electronic Testing: Theory and Applications*, vol. 16, no. 5, Oct. 2000, pp 463-476, M. A. Gharaybeh*, V. D. Agrawal, M. L. Bushnell, and C. G. Parodi*.
5. "Path Delay Fault Simulation of Sequential Circuits," *IEEE Trans. on Computer-Aided Design*, vol. 8, no. 2, April, 2000, pp 223-228, T. J. Chakraborty*, V. D. Agrawal, and M. L. Bushnell.
6. "Effect of Noise on Analog Circuit Testing," accepted for the special issue on the *1998 VLSI Test Symposium, Journal of Electronic Testing: Theory and Applications*, vol 15, no. 1/2, Aug./Oct. 1999, pp 11-22, M. K. Iyer* and M. L. Bushnell.
7. "Test Generation for Mixed-Signal Devices Using Signal Flow Graphs," *Journal of Electronic Testing: Theory and Applications*, vol. 14, no. 3, July, 1999, pp 189-205, M. L. Bushnell and R. Ramadoss*.
8. "A Parallel-Vector Concurrent-Fault Simulator and Generation of Single-Input Change Tests for Path Delay Faults," *IEEE Trans. on Computer-Aided Design*, vol. 17, no. 9, Sept. 1998, pp 83-86, M. A. Gharaybeh*, M. L. Bushnell, and V. D. Agrawal.
9. "Statistical Delay Fault Coverage Estimation for Synchronous Sequential Circuits," *Journal of Electronic Testing: Theory and Applications*, vol. 3, no. 3, June 1998, pp 239-254, L. Pappu*, M. L. Bushnell, V. D. Agrawal, and S. Mandyam-Komar.
10. "The Path Status Graph with Application to Delay Fault Simulation," *IEEE Trans. on Computer-Aided Design*, vol. 17, no. 4, April 1998, pp 324-332, M. A. Gharaybeh*, M. L. Bushnell, and V. D. Agrawal.
11. "On Variable Clock Methods for Path Delay Testing of Sequential Circuits," *IEEE Trans. on Computer-Aided Design*, vol. 16, no. 11, Nov. 1997, pp 1237-1249, T. J. Chakraborty*, V. D. Agrawal, and M. L. Bushnell.
12. "Classification and Test Generation for Path-Delay Faults Using Single Stuck-at Fault Tests," *Journal of Electronic Testing: Theory and Applications*, vol. 11 no. 1, Aug. 1997, pp 55-67, M. A. Gharaybeh*, M. L. Bushnell, and V. D. Agrawal.
13. "Improving a Nonenumerative Method to Estimate Path Delay Fault Coverage," *IEEE Trans. on Computer-Aided Design*, vol. 16, no. 7, July 1997, pp 759-762, K. Heragu*, V. D. Agrawal, M. L. Bushnell, and J. H. Patel.
14. "A Functional Decomposition Method for Redundancy Identification and Test Generation," *Journal of Electronic Testing: Theory and Applications*, vol. 10, no. 3, June 1997, pp 175-195, M. L. Bushnell and J. Giraldi*.

15. "Sequential Circuit Test Generation Using Dynamic Justification Equivalence," *Journal of Electronic Testing: Theory and Applications*, vol. 8, no. 1, Feb. 1996, pp 9-33, X. Chen* and M. L. Bushnell.
16. "Fault Coverage Estimation by Test Vector Sampling," *IEEE Trans. on Computer-Aided Design*, vol. 14, no. 5, May 1995, pp 590-596, K. Heragu*, V. D. Agrawal, and M. L. Bushnell.
17. "Energy Minimization and Design for Testability," *Journal of Electronic Testing: Theory and Applications*, vol. 5, no. 1, Feb. 1994, pp 57-66, S. T. Chakradhar*, V. D. Agrawal, and M. L. Bushnell. Also issued as AT&T Bell Laboratories Technical Memorandum # 11273-900814-05TM.
18. "A Solvable Class of Quadratic 0-1 Programming," *Journal of Discrete Applied Mathematics*, vol. 36, no. 3, May 1992, pp 233-251, S. T. Chakradhar* and M. L. Bushnell.
19. "Test Generation Using Neural Computers," *Int'l. Journal of Computer-Aided VLSI Design*, vol. 3, no. 3, 1991, pp 241-257, S. T. Chakradhar*, V. D. Agrawal, and M. L. Bushnell. Also issued as AT&T Bell Laboratories Technical Memorandum # 11273-900816-07TM.
20. "Neural Net and Boolean Satisfiability Models of Logic Circuits," *IEEE Design and Test of Computers*, vol. 7, no. 5, Oct. 1990, pp 54-57, S. T. Chakradhar*, V. D. Agrawal, and M. L. Bushnell.
21. "Toward Massively Parallel Automatic Test Generation," *IEEE Trans. on Computer-Aided Design*, vol. 9, no. 9, Sept. 1990, pp 981-994, S. T. Chakradhar*, M. L. Bushnell, and V. D. Agrawal. Also issued as AT&T Bell Laboratories Technical Memorandum # 11273-900814-03TM.
22. "Automated Design Tool Execution in the *Ulysses* Design Environment," *IEEE Trans. on Computer-Aided Design*, vol. 8, no. 3, March 1989, pp 279-287, M. L. Bushnell and S. W. Director.
23. "ULYSSES – A Knowledge Based VLSI Design Environment," *Int'l. Journal for Artificial Intelligence in Engineering*, vol. 2, no. 1, Jan. 1987, pp 34-41, M. L. Bushnell and S. W. Director.
24. "DIF: A Framework for VLSI Multi-Level Representation," *INTEGRATION, The VLSI Journal*, vol. 2, no. 3, Sept. 1984, pp 227-241, D. P. LaPotin, S. R. Nassif, J. V. Rajan, M. L. Bushnell, and J. A. Nestor.
25. "Computerized Thermal Mechanical Fatigue Testing," *Industrial Research*, vol. 19, no. 7, July 1977, pp 60-64, M. L. Bushnell and J. J. Martin.

Journal Articles (not refereed):

1. "Guest Editorial," *Int'l. Journal for Artificial Intelligence in Engineering*, vol. 1, no. 2, Oct. 1986, pp 67-69, by M. L. Bushnell and P. Haren.

Refereed Electronic Publications:

(Graduate Students supervised indicated by *, Undergraduate Students by **)

1. "An Exact Non-Enumerative Fault Simulator for Path-Delay Faults," *Proc. of TECHCON '96*, Semiconductor Research Corporation, Phoenix, Arizona, (http://www.src.org/resrch/pubs/pubs96/toc/un_022.dgw), Sept. 12-14 1996, 10 p., M. A. Gharaybeh*, M. L. Bushnell, and V. D. Agrawal.

Refereed Conference Papers in Proceedings:

(Graduate Students supervised indicated by *, Undergraduate Students by **)

1. "A Novel Dynamic Power Cutoff Technique (DPCT) for Active Leakage Reduction in Deep Submicron CMOS Circuits," *International Symposium on Low-Power Electronics and Design*, Oct. 2006, pp 214-219, Baozhen Yu* and Michael L. Bushnell.
2. "Zero Cost Test Point Insertion Technique for Structured ASICs," *20th International Conference on VLSI Design*, Jan. 2007, Rajamani Sethuram*, Seongmoon Wang, Srimat T. Chakradhar, and M. L. Bushnell.
3. "Test Pattern Generation Using Modulation by Haar Wavelets and Correlation for Sequential BIST," *20th International Conference on VLSI Design*, Jan. 2007, Suresh K. Devanathan* and M. L. Bushnell.
4. "Analog Circuit Testing Using Auto Regressive Moving Average (ARMA) Models," *20th International Conference on VLSI Design*, Jan. 2007, Jeff Ayres* and M. L. Bushnell.
5. "Architecture for Variable-Length Combined FFT, DCT, and MWT Transform Hardware for a Multi-Mode Wireless System," *20th International Conference on VLSI Design*, Jan. 2007, Rohit Pandey* and M. L. Bushnell.
6. "Fault Models and Device Yield of a Large Population of Room Temperature Operation Single-Electron Transistors," *20th International Conference on VLSI Design*, Jan. 2007, Dan Mazor*, M. L. Bushnell, David J. Mulligan*, and Richard J. Blaikie.
7. "Power Reduction Using a Novel Neural Net Branch Predictor," *20th International Conference on VLSI Design*, Jan. 2007, Rajamani Sethuram*, Hari Vijay Venkatanarayanan*, Omar Khan*, and M. L. Bushnell.
8. "An Area Efficient Mixed-Signal Test Architecture for Systems-on-a-Chip," *19th International Conference on VLSI Design*, Jan. 2006, pp 161-168, Hari V. Venkatanarayanan* and M. L. Bushnell, winner of the *N. N. Biswas Best Student Paper Prize*.
9. "Sequential Spectral ATPG Using the Wavelet Transform and Compaction," *19th International Conference on VLSI Design*, Jan. 2006, pp 407-412, Suresh K. Devanathan* and M. L. Bushnell.
10. "Automatic Path-Delay Fault Test Generation for Combined Resistive Vias, Resistive Bridges, and Capacitive Crosstalk Delay Faults," *19th International Conference on VLSI Design*, Jan. 2006, pp 413-418, Shweta Chary* and M. L. Bushnell.
11. "Aliasing Analysis of Spectral Statistical Response Compaction Techniques," *19th International Conference on VLSI Design*, Jan. 2006, pp 801-806, Omar I. Khan* and M. L. Bushnell.
12. "Analog Macromodeling for Combined Resistive Vias, Resistive Bridges, and Capacitive Crosstalk Delay Faults," *19th International Conference on VLSI Design*, Jan. 2006, pp 818-823, Shweta Chary* and M. L. Bushnell.
13. "Design of Variable Input Delay Gates for Low Dynamic Power Circuits," *International Workshop on Power and Timing Modeling, Optimization, and Simulation (PATMOS)*, 2005, pp 436-445, T. Raja*, V. D. Agrawal, and M. L. Bushnell.

14. "Glitch-Free Design of Low Power ASICs Using Customized Resistive Feedthrough Cells," *VLSI Design and Test Symposium*, India, Aug. 2005, pp 41-49, S. Uppalapati*, M. L. Bushnell, and V. D. Agrawal.
15. "Variable Input Delay CMOS Logic for Low-Power Design," *Int'l. Conf. on VLSI Design*, India, Jan. 2005, pp 598-605, T. Raja*, V. D. Agrawal, and M. L. Bushnell.
16. "Using Contrapositive Law in an Implication Graph," *Int'l. Conf. on VLSI Design*, India, Jan. 2005, pp 723-729, K. K. Dave*, V. D. Agrawal, and M. L. Bushnell.
17. "Spectral Analysis for Statistical Response Compaction During Built-In Self-Testing," *Int'l. Test Conf.*, Oct., 2004, pp 67-76, O. Khan* and M. L. Bushnell.
18. "On Random Pattern Generation with the Selfish Gene Algorithm for Testing Digital Sequential Circuits," *Int'l. Test Conf.*, Oct., 2004, pp 617-626, J. Zhang*, M. L. Bushnell, and V. D. Agrawal.
19. "Using Contrapositives to Enhance the Implication Graphs of Logic Circuits," *North Atlantic Test Workshop*, May, 2004, pp 56-63, K. Dave* and V. D. Agrawal and M. L. Bushnell.
20. "A Tutorial on the Emerging Nanotechnology Devices," 2004 *Int'l. Conf. on VLSI Design*, January, 2004, pp 343-360, T. V. Raja*, V. D. Agrawal, and M. L. Bushnell.
21. "CMOS Circuit Design for Minimum Dynamic Power and Highest Speed," 2004 *Int'l. Conf. on VLSI Design*, January, 2004, pp 1035-1040, T. V. Raja*, V. D. Agrawal, and M. L. Bushnell.
22. "New Graphical I_{DDQ} Signatures Reduce Defect Level and Yield Loss", *Int'l. Conf. on VLSI Design*, January, 2003, pp 353-360, L. Rao*, M. L. Bushnell, and V. D. Agrawal.
23. "A Fault-Independent Transitive Closure Algorithm for Redundancy Identification", *Int'l. Conf. on VLSI Design*, January, 2003, pp 149-154, V. Mehta*, K. Dave*, V. D. Agrawal, and M. L. Bushnell.
24. "Minimum Dynamic Power CMOS Circuit Design by a Reduced Constraint Set Linear Program", 2003 *Int'l. Conf. on VLSI Design*, January, 2003, pp 527-532, T. V. Raja*, V. D. Agrawal, and M. L. Bushnell.
25. "Analog Macromodeling of Capacitive Coupling Faults in Digital Circuit Interconnects," 2002 *International Test Conference*, October, 2002, pp 375-383, A. D. Sathe*, M. L. Bushnell, and V. D. Agrawal.
26. "Minimum Dynamic Power Design of CMOS Circuits by Linear Program Using a Reduced Constraint Set", 2002 *VLSI Design and Test Workshop*, August, 2002, T. V. Raja*, V. D. Agrawal, and M. L. Bushnell, Bangalore, India.
27. "Digital Spectral Test Generation for Mixed-Signal Circuit Testing," *North Atlantic Test Workshop*, May, 2002, pp 92-100, A. Bisaria* and M. L. Bushnell.
28. "Analog Macromodeling of Capacitive Coupling Faults in Digital Circuit Interconnects," *North Atlantic Test Workshop*, May, 2002, pp 56-66, A. D. Sathe*, M. L. Bushnell, and V. D. Agrawal.

29. "New Graphical I_{DDQ} Signatures Reduce Defect Level and Yield Loss," *North Atlantic Test Workshop*, May, 2002, pp 45-55, L. Rao*, M. L. Bushnell, and V. D. Agrawal.
30. "A New Transitive Closure Algorithm with Application to Redundancy Identification," *1st IEEE International Workshop on Electronics Design, Test & Applications (DELTA 2002)*, Jan. 2002, pp 496-500, Christ Church, New Zealand, V. Gaur*, V. D. Agrawal, and M. L. Bushnell.
31. "A Code Transition Delay Fault Model for A/D Converter Testing," *14th Int'l. Conf. on VLSI Design (VLSI Design '01)*, Bangalore, India, Jan. 2001, pp 274-282, S. Mohan* and M. L. Bushnell.
32. "Digital Circuit Design for Minimum Transient Energy and a Linear Programming Method," *12th Int'l. Conf. on VLSI Design (VLSI Design '99)*, Goa, India, Jan. 1999, pp 434-439, V. D. Agrawal, M. L. Bushnell, G. Parthasarathy*, and R. Ramadoss*.
33. "A Complete Characterization of Path Delay Faults through Stuck-At Faults," *12th Int'l. Conf. on VLSI Design (VLSI Design '99)*, Goa, India, Jan. 1999, pp 492-497, S. Majumder*, B. B. Bhattacharya, V. D. Agrawal, and M. L. Bushnell.
34. "False-Path Removal Using Delay Fault Simulation," *Seventh Asian Test Symposium*, Dec. 1998, pp 82-87, M. A. Gharaybeh*, V. D. Agrawal, and M. L. Bushnell.
35. "A Non-Enumerative Path Delay Fault Simulator for Sequential Circuits," *1998 IEEE International Test Conference*, Oct. 1998, pp 934-943, C. G. Parodi*, V. D. Agrawal, M. L. Bushnell, and S. Wu.
36. "Random Logic Partial-Scan Delay-Fault Built-In Self-Test," invited paper, *1998 IMAPS and IEEE Advanced Technology Workshop on Multi-Chip Module Test V*, Sept. 1998, pp 29-30, M. L. Bushnell and G. Parthasarathy*.
37. "Test Generation for Analog Circuits Using Partitioning and Inverted System Simulation," *4th IEEE International Mixed-Signal Testing Workshop*, The Hague, The Netherlands, June 8-11 1998, pp 68-73, R. Ramadoss* and M. L. Bushnell.
38. "Effect of Noise on Analog Circuit Testing," *16th IEEE VLSI Test Symposium*, Monterey, CA, April 26-30 1998, pp 138-144, M. K. Iyer* and M. L. Bushnell.
39. "Towards Simultaneous Delay-Fault Built-In Self-Test and Partial-Scan Insertion," *16th IEEE VLSI Test Symposium*, Monterey, CA, April 26-30 1998, pp 210-217, G. Parthasarathy* and M. L. Bushnell.
40. "On Delay-Untestable Paths and Stuck-Fault Redundancy," *16th IEEE VLSI Test Symposium*, Monterey, CA, April 26-30 1998, pp 194-199, S. Majumder*, V. D. Agrawal, and M. L. Bushnell.
41. "Path Delay Testing: Variable-Clock Versus Rated-Clock," *11th Int'l. Conf. on VLSI Design (VLSI Design '98)*, Chennai, India, Jan. 4-7 1998, pp 470-475, S. Majumder*, V. D. Agrawal, and M. L. Bushnell.
42. "Flash A/D Converters – Design for Testability," *3rd IEEE International Mixed-Signal Testing Workshop*, Seattle, Washington, June 3-6 1997, pp 62-67, R. Ramadoss* and M. L. Bushnell.

43. "Flags and Algebra for Sequential Circuit VNR Path Delay Fault Test Generation," *10th Int'l. Conf. on VLSI Design (VLSI Design '97)*, Hyderabad, India, Jan. 4-7 1997, pp 88-94, M. K. Srinivas, M. L. Bushnell, and V. D. Agrawal.
44. "Redundancy Identification Using Transitive Closure," *Fifth Asian Test Symposium*, Hsinchu, Taiwan, Nov. 20-22 1996, pp 4-9, V. D. Agrawal, M. L. Bushnell, and Q. Lin*.
45. "An Exact Non-Enumerative Fault Simulator for Path-Delay Faults," *1996 IEEE International Test Conference*, Washington, D.C., Oct. 20-25 1996, pp 276-285, M. A. Gharaybeh*, M. L. Bushnell, and V. D. Agrawal.
46. "Built-In and External Test of Known Good Die for Mixed Signal Modules," *Proceedings of DARPA Electronic Packaging and Interconnect Design and Test Program Review*, Herndon, Virginia, April 30-May 2 1996, pp 89-97, M. L. Bushnell.
47. "Test Generation for Mixed-Signal Devices Using Signal Flow Graphs," *Proceedings of DARPA Electronic Packaging and Interconnect Design and Test Program Review*, Herndon, Virginia, April 30-May 2 1996, pp 98-105, R. Ramadoss* and M. L. Bushnell.
48. "Test Generation for Mixed-Signal Devices Using Signal Flow Graphs," *9th Int'l. Conf. on VLSI Design (VLSI Design '96)*, Bangalore, India, Jan. 3-6 1996, pp 242-248, R. Ramadoss* and M. L. Bushnell, winner of the *Honorable Mention Award*.
49. "Statistical Path-Delay Fault Coverage Estimation for Synchronous Sequential Circuits," *9th Int'l. Conf. on VLSI Design (VLSI Design '96)*, Bangalore, India, Jan. 3-6 1996, pp 290-295, L. Pappu*, M. L. Bushnell, V. D. Agrawal, and M. K. Srinivas.
50. "Parallel Concurrent Path-Delay Fault Simulation Using Single-Input Change Patterns," *9th Int'l. Conf. on VLSI Design (VLSI Design '96)*, Bangalore, India, Jan. 3-6 1996, pp 426-431, M. A. Gharaybeh*, M. L. Bushnell, and V. D. Agrawal, nominated for a *Best Paper Award*.
51. "Functional Test Generation for Path Delay Faults," *Fourth Asian Test Symposium*, Bangalore, India, Nov. 23-24 1995, pp 339-345, M. K. Srinivas, V. D. Agrawal, and M. L. Bushnell.
52. "Classification and Test Generation for Path-Delay Faults Using Single Stuck-Fault Tests," *1995 IEEE International Test Conference*, Washington, D.C., Oct. 21-25 1995, pp 139-148, M. A. Gharaybeh*, M. L. Bushnell, and V. D. Agrawal.
53. "An Adaptive Distributed Algorithm for Sequential Circuit Test Generation," *Proceedings of European Design Automation Conference (EURO-DAC '95)*, Sept. 1995, pp 236-241, J. Sienicki*, M. L. Bushnell, P. Agrawal, and V. D. Agrawal.
54. "Circuit Design for Low Overhead Delay-Fault BIST Using Constrained Quadratic 0-1 Programming," *13th IEEE VLSI Test Symposium*, Princeton, N. J., April 30-May 3 1995, pp 393-399, I. P. Shaik* and M. L. Bushnell.
55. "An Asynchronous Algorithm for Sequential Circuit Test Generation on a Network of Workstations," nominated for a *Best Paper Award*, *8th Int'l. Conf. on VLSI Design (VLSI Design '95)*, New Delhi, India, Jan. 4-7 1995, pp 36-41, J. Sienicki*, M. L. Bushnell, P. Agrawal, and V. D. Agrawal.

56. "Generalization of Search State Equivalence for Automatic Test Pattern Generation," *8th Int'l. Conf. on VLSI Design (VLSI Design '95)*, New Delhi, India, Jan. 4-7 1995, pp 99-103, X. Chen* and M. L. Bushnell.
57. "Statistical Methods for Delay Fault Coverage Analysis," *8th Int'l. Conf. on VLSI Design (VLSI Design '95)*, New Delhi, India, Jan. 4-7 1995, pp 166-170, K. Heragu*, V. D. Agrawal, and M. L. Bushnell.
58. "A Graph Approach to DFT Hardware Placement for Robust Delay Fault BIST," *8th Int'l. Conf. on VLSI Design (VLSI Design '95)*, New Delhi, India, Jan. 4-7 1995, pp 177-182, I. P. Shaik* and M. L. Bushnell.
59. "Superlinear Speedup in Multiprocessing Environment," *The First International Workshop on Parallel Processing*, Bangalore, India, Dec. 1994, pp 261-265, P. Agrawal, V. D. Agrawal, M. L. Bushnell, and J. Sienicki*.
60. "Rapid Application-Specific Electronic Module Design and Test," *Proceedings of Advanced Research Projects Agency Application-Specific Electronic Modules Conference*, Poughkeepsie, New York, Sept. 28-30 1994, pp 281-292, M. L. Bushnell.
61. "Dynamic State and Objective Learning for Sequential Circuit Automatic Test Generation using Decomposition Equivalence," *Twenty-Fourth IEEE Annual International Symposium on Fault-Tolerant Computing - FTCS-24*, Austin, Texas, June 15-17 1994, pp 446-455, X. Chen* and M. L. Bushnell.
62. "An Efficient Path Delay Fault Coverage Estimator," *31st ACM/IEEE Design Automation Conference*, San Diego, CA, June 6-10 1994, pp 516-521, K. Heragu*, M. L. Bushnell, and V. D. Agrawal. Also issued as CAIP Research Center Technical Report # CAIP-TR-170.
63. "FACTS: Fault Coverage Estimation by Test Vector Sampling," *12th IEEE VLSI Test Symposium*, Cherry Hill, NJ, April 25-28 1994, pp 266-271, K. Heragu*, V. D. Agrawal, and M. L. Bushnell.
64. "Neural Models for Transistor and Mixed-Level Test Generation," *12th IEEE VLSI Test Symposium*, Cherry Hill, NJ, April 25-28 1994, pp 208-213, C. L. C. Cooper* and M. L. Bushnell.
65. "Distributed Computing, Automatic Design, and Error Recovery in the Ulysses II Framework," *European Design and Test Conference - 1994*, (EDAC-ETC-EUROASIC) Paris, France, Feb. 28-March 3 1994, pp 610-617, S. Parikh*, M. L. Bushnell, J. Sienicki*, and R. Ganesh*. Also issued as CAIP Research Center Technical Report # CAIP-TR-169.
66. "Rapid Application-Specific Electronic Module Design and Test," *Proceedings of Advanced Research Projects Agency Electronic Packaging and Interconnect Meeting (EPI)*, Marina Del Ray, CA, Feb. 14-18 1994, vol. 1, paper 17, M. L. Bushnell.
67. "Graphical Methodology Language for CAD Frameworks" *7th Int'l. Conf. on VLSI Design (VLSI Design '94)*, Calcutta, India, Jan. 5-8 1994, pp 401-406, J. Sienicki*, M. L. Bushnell, and S. Parikh*.
68. "Distributed Gentest," *The 12th AT&T Conference on Electronic Testing*, Sept. 27-28 1993, pp 285-294, J. Sienicki*, P. Agrawal, M. L. Bushnell, and V. D. Agrawal.

69. "Design for Testability for Path Delay Faults in Sequential Circuits," *30th ACM/IEEE Design Automation Conference*, Dallas, TX, June 14-18 1993, pp 453-457, T. J. Chakraborty*, V. D. Agrawal, and M. L. Bushnell.
70. "New Methods for Delay Fault Testing of Sequential Circuits," *The 11th AT&T Conference on Electronic Testing*, Princeton, NJ, Oct. 26-27 1992, pp 1.3.1-1.3.10, T. J. Chakraborty*, V. D. Agrawal, and M. L. Bushnell.
71. "Delay Fault Models and Test Generation for Random Logic Sequential Circuits," *29th ACM/IEEE Design Automation Conference*, Anaheim, CA, June 8-12 1992, pp 165-172, T. J. Chakraborty*, V. D. Agrawal, and M. L. Bushnell, nominated for a *Best Paper Award*.
72. "Path Delay Fault Simulation Algorithms for Sequential Circuits," *First Asian Test Symposium*, Nov. 26-28 1991, pp 51-56, T. J. Chakraborty*, V. D. Agrawal, and M. L. Bushnell.
73. "Search State Equivalence for Redundancy Identification and Test Generation," *1991 IEEE International Test Conference*, Nashville, TN, Oct. 26-30 1991, pp 184-193, J. Giraldi* and M. L. Bushnell.
74. "EST: The New Frontier in Automatic Test-Pattern Generation," *27th ACM/IEEE Design Automation Conference*, Orlando, FL, June 24-28 1990, pp 667-672, J. Giraldi* and M. L. Bushnell.
75. "Automatic Test Generation Using Quadratic 0-1 Programming," *27th ACM/IEEE Design Automation Conference*, Orlando, FL, June 24-28 1990, pp 654-659, S. T. Chakradhar*, V. D. Agrawal, and M. L. Bushnell, one of 15 papers nominated for a *Best Paper Award*.
76. "Polynomial Time Solvable Fault Detection Problems," *Twentieth IEEE Annual International Symposium on Fault-Tolerant Computing*, Newcastle Upon Tyne, UK, June 26-28 1990, pp 56-63, S. T. Chakradhar*, V. D. Agrawal, and M. L. Bushnell.
77. "MHERTZ: A New Optimization Algorithm for Floorplanning and Global Routing," *27th ACM/IEEE Design Automation Conference*, Orlando, FL, June 24-28 1990, pp 107-110, D. R. Brasen* and M. L. Bushnell.
78. "Automatic Test Generation Using Neural Networks," *IEEE International Conference on Computer-Aided Design*, Nov. 7-10 1988, pp 416-419, S. T. Chakradhar*, M. L. Bushnell, and V. D. Agrawal, *Used for Conference Publicity (Best Testing Paper)*.
79. "A Module Area Estimator for VLSI Layout," *25th ACM/IEEE Design Automation Conference*, Anaheim, CA, June 12-15 1988, pp 54-59, X. Chen* and M. L. Bushnell.
80. "VLSI CAD Tool Integration Using the ULYSSES Environment," *23rd ACM/IEEE Design Automation Conference*, Las Vegas, Nevada, June 29-July 2 1986, pp 55-61, M. L. Bushnell and S. W. Director.
81. "A Software Driver for a Real-Time Laboratory Automation System," *ASTM Symposium on Automated Materials Testing*, Philadelphia, PA, Nov. 5-11 1978, published in *Computer Automation of Materials Testing*, Special Technical Publication 710, American Society for Testing and Materials, 1980, pp 26-47, M. L. Bushnell and L. K. Sisterson, B. C. Wonsiewicz, editor.

Non-Refereed Conference Papers in Proceedings:

(Graduate Students supervised indicated by *, Undergraduate Students by **)

1. "Fabrication and Characterisation of Silicon Single Electron Transistors," *Proc. of the 11th Electronics New Zealand Conf. (ENZCON '04)*, Nov. 2004, pp 1-6, R. J. Blaikie, **D. J. Mulligan, **H.-Y. Chen, *D. Mazor, and M. L. Bushnell.

Technical Reports:

(Graduate Students supervised indicated by *, Undergraduate Students by **)

1. *A Graph Approach to DFT Hardware Placement for Robust Delay Fault Built-In Self-Testing*, Center for Computer Aids for Industrial Productivity, Rutgers University, Technical Report CAIP-TR-94, 15 pp., Sept. 26 1994, I. P. Shaik* and M. L. Bushnell.
2. *Automatic Circuit Redesign for Delay Fault Testability Using Constrained Quadratic 0-1 Programming*, Center for Computer Aids for Industrial Productivity, Rutgers University, Technical Report CAIP-TR-193, 16 pp., Sept. 26 1994, I. P. Shaik* and M. L. Bushnell.
3. *An Efficient Path Delay Fault Coverage Estimator*, Center for Computer Aids for Industrial Productivity, Rutgers University, Technical Report CAIP-TR-170, 13 pp., Nov. 8 1993, K. Heragu*, M. L. Bushnell, and V. D. Agrawal.
4. *Justification State Equivalence for Sequential Circuit Automatic Test Generation*, Center for Computer Aids for Industrial Productivity, Rutgers U., Technical Report CAIP-TR-173, 20 pp., Nov. 8 1993, X. Chen* and M. L. Bushnell.
5. *Automatic Switch-Level Test Generation Using Energy Minimization*, Center for Computer Aids for Industrial Productivity, Rutgers U., Technical Report CAIP-TR-172, 17 pp., Nov. 8 1993, C. L. C. Cooper* and M. L. Bushnell.
6. *A Robust Delay Fault Built-In Self-Testing Model*, Center for Computer Aids for Industrial Productivity, Rutgers U., Technical Report CAIP-TR-171, 15 pp., Nov. 8 1993, I. P. Shaik* and M. L. Bushnell.
7. *Distributed Computing, Automatic Design, and Error Recovery in the Ulysses II Framework*, Center for Computer Aids for Industrial Productivity, Rutgers University, Technical Report CAIP-TR-169, 22 pp., Oct. 29 1993, S. Parikh*, M. L. Bushnell, J. Sienicki*, and R. Ganesh*.
8. *Statistical Estimation of Delay Fault Coverage*, Center for Computer Aids for Industrial Productivity, Rutgers U., Technical Report CAIP-TR-168, 10 pp., Oct. 22 1993, K. Heragu*, V. D. Agrawal, and M. L. Bushnell.
9. *Search State Equivalence for Redundancy Identification and Test Generation*, Center for Computer Aids for Industrial Productivity, Rutgers University, Technical Report CAIP-TR-131, 16 pp., April 2 1991, J. Giralidi* and M. L. Bushnell.
10. *On Test Generation Using Neural Computers*, AT&T Bell Laboratories Technical Memorandum # 11273-900816-07TM, 19 pp., Aug. 16 1990, S. T. Chakradhar*, V. D. Agrawal, and M. L. Bushnell.
11. *Energy Minimization and Design for Testability*, AT&T Bell Laboratories Technical Memorandum # 11273-900814-05TM, 18 pp., Aug. 14 1990, S. T. Chakradhar*, V. D. Agrawal, and M. L. Bushnell.

12. *A Discrete Non-Linear Optimization Method for Test Generation*, AT&T Bell Laboratories Technical Memorandum # 11273-900814-04TM, 17 pp., Aug. 14 1990, S. T. Chakradhar*, V. D. Agrawal, and M. L. Bushnell.
13. *The New Frontier in Automatic Test-Pattern Generation* – Center for Computer Aids for Industrial Productivity, Rutgers U., Technical Report CAIP-TR-112, 20 pp., Feb. 15 1990, J. Giraldi* and M. L. Bushnell.
14. *Polynomial Time Solvable Fault Detection Problems* – Center for Computer Aids for Industrial Productivity, Rutgers U., Technical Report CAIP-TR-111, 20 pp., Feb. 15 1990, S. T. Chakradhar*, V. D. Agrawal, and M. L. Bushnell.
15. *Automatic Test Generation Using Quadratic 0-1 Programming* – Center for Computer Aids for Industrial Productivity, Rutgers U., Technical Report CAIP-TR-110, 20 pp., Feb. 15 1990, S. T. Chakradhar*, V. D. Agrawal, and M. L. Bushnell.
16. *Automated Design Tool Execution in the Ulysses Design Environment*, Center for Computer Aids for Industrial Productivity, Rutgers University, Technical Report CAIP-SR-008, 28 pp., Feb. 15 1990, M. L. Bushnell and S. W. Director.
17. *Towards Massively Parallel Automatic Test Generation* – Center for Computer Aids for Industrial Productivity, Rutgers U., Technical Report CAIP-TR-084, 22 pp., Oct. 11 1988, S. T. Chakradhar*, M. L. Bushnell, and V. D. Agrawal.
18. *Towards Massively Parallel Automatic Test Generation* – AT&T Bell Laboratories Technical Memorandum # 11273-900814-03TM, 31 pp., Aug. 14 1990, S. T. Chakradhar*, M. L. Bushnell, and V. D. Agrawal.
19. *A Solvable Class of Quadratic 0-1 Programming* – Center for Computer Aids for Industrial Productivity, Rutgers U., Technical Report CAIP-TR-081, 16 pp., Oct. 10 1988, S. T. Chakradhar* and M. L. Bushnell.
20. *MAE – A Module Area Estimator for VLSI Layout* – Center for Computer Aids for Industrial Productivity, Rutgers U., Technical Report CAIP-SR-007, 79 pp., Sept. 1988, X. Chen* and M. L. Bushnell.
21. *Automatic Test Generation Using Neural Networks* – Center for Computer Aids for Industrial Productivity, Rutgers U., Technical Report CAIP-TR-078, 13 pp., July 15 1988, S. T. Chakradhar*, M. L. Bushnell, and V. D. Agrawal.
22. *Automatic Test Generation Using Neural Networks* – AT&T Bell Laboratories Technical Memorandum # 11273-880830-04TM, 12 pp., Aug. 30 1988, S. T. Chakradhar*, M. L. Bushnell, and V. D. Agrawal.
23. *A Module Area Estimator for VLSI Layout* – Center for Computer Aids for Industrial Productivity, Rutgers U., Technical Report CAIP-TR-064, 34 pp., Feb. 11 1988, X. Chen* and M. L. Bushnell.
24. *Computer Aided Pad Layout Enhancement Tool* – Center for Computer Aids for Industrial Productivity, Rutgers U., Technical Report CAIP-TR-063, 34 pp., Feb. 11 1988, D. Lee** and M. L. Bushnell.

25. *Automated Design Tool Execution in the Ulysses Design Environment*, SRC-Carnegie Mellon U. Research Center for CAD, Research Report CMUCAD-88-4, 9 pp., Jan. 1988, M. L. Bushnell and S. W. Director.
26. *ULYSSES Design Environment User's Guide* – SRC-Carnegie Mellon U. Research Center for CAD, Research Report CMUCAD-87-16, 134 pp., May 1987, M. L. Bushnell.
27. *ULYSSES – An Expert-System Based VLSI Design Environment* – SRC-Carnegie Mellon U. Research Center for CAD, Research Report CMUCAD-87-15, 236 pp., May 1987, M. L. Bushnell.
28. *Framesmith Data Base Access Functions and User's Manual* – SRC-Carnegie Mellon U. Research Center for CAD, Research Report CMUCAD-85-68, 28 pp., Dec. 1985, M. L. Bushnell.
29. *DIF: The CMU-DA Intermediate Form* – SRC-Carnegie Mellon U. Research Center for CAD, Research Report CMUCAD-83-20, 15 pp., 1983, D. P. LaPotin, S. R. Nassif, J. V. Rajan, M. L. Bushnell, and J. A. Nestor.
30. Master's Thesis: *DELILAH II – An Enhanced Menu-Driven Input Processor*, SRC-Carnegie Mellon U. Research Center for CAD, Research Report CMUCAD-83-7, 147 pp., Feb. 1983, M. L. Bushnell.

Reviews:

1. Review of chapter 8 of the text, *Algorithms*, by Robert Sedgewick, of Princeton University, for Addison-Wesley Benjamin/Cummings, April 1989, by M. L. Bushnell.

Invited Presentations (Graduate Students supervised indicated by *, Undergraduate Students by **)

1. Invited Lecture, *System Fault-Tolerance and Testing Models for Nanotechnology*, ECE Dept., U. of Waterloo, Waterloo, Ontario, Dec. 10, 2004.
2. Invited Lecture, *System Fault-Tolerance and Testing Models for Nanotechnology*, Intel Corp. Test Review, Santa Clara, CA, Nov. 2004.
3. Paid Tutorial: *Essentials of Electronic Testing*, GlobespanVirata, New Jersey, Nov. 6-7, 2003, M. L. Bushnell.
4. Invited Lecture, *Trends in ULSI Circuit (ULSI) Technology for the Next 15 Years*, the IEEE, Christchurch, New Zealand, October 9, 2003, M. L. Bushnell.
5. *Spectral Test Pattern Generation for Built-In Self-Test of Sequential Circuits*, University of Canterbury, Christchurch, New Zealand, August 22, 2003.
6. Paid Conference Tutorial: *Essentials of Electronic Testing, 2001 VLSI Test Symposium*, Los Angeles, CA, April-May, 2001, V. D. Agrawal and M. L. Bushnell.
7. Paid Conference Tutorial: *Essentials of Electronic Testing, 2001 VLSI Test Symposium*, Bangalore, India, Jan., 2002, V. D. Agrawal and M. L. Bushnell.
8. "A Code Transition Delay Fault Model for A/D Converter Testing," Indian Institute of Technology, Chennai, India, January 12, 2001, M. L. Bushnell.

9. "A Code Transition Delay Fault Model for A/D Converter Testing," Accel Technologies, Ltd., Chennai, India, January 12, 2001, M. L. Bushnell.
10. "Partial-Scan Delay-Fault Built-In Self-Test of Large Circuits," Lucent Microelectronics, Allentown, PA, March 20 1998, M. L. Bushnell.
11. "Automatic Test-Pattern Generation for Mixed Signal Circuits," *DARPA Electronic Packaging and Interconnects Conference*, San Diego, CA, March 1998, M. L. Bushnell.
12. "Systems Testing," invited paper, *IEEE Computer Society 1997 Annual Workshop on VLSI*, Orlando, Florida, Nov. 3-6 1997, M. L. Bushnell.
13. "Minimum Observable Signal Variation: A New Mixed-Signal Fault Model," Poster, *3rd IEEE International Mixed-Signal Testing Workshop*, Seattle, Washington, June 3-6 1997, R. Ramadoss*, M. L. Bushnell, and V. D. Agrawal.
14. "Markov Chain Based Sequential Automatic Test Pattern Generator," *1997 Test Synthesis Workshop*, May 4-5 1997, L. Pappu*, M. L. Bushnell, and V. D. Agrawal.
15. "Future Directions in Sequential Automatic Test-Pattern Generation," invited paper, *IEEE Computer Society 1996 Annual Workshop on VLSI*, Clearwater, Florida, Nov. 3-6 1996, M. L. Bushnell.
16. "Automatic Test-Pattern Generation for Mixed Signal Circuits," *DARPA Electronic Packaging and Interconnect Conference*, Washington, DC, Oct. 1996, M. L. Bushnell.
17. "Test Generation for Mixed-Signal Devices Using Signal Flow Graphs," U. of Washington, Seattle, July 1996, M. L. Bushnell.
18. "Advanced Algorithms for Automatic Test-Pattern Generation," *Semiconductor Research Corporation, Joint Test Review*, U. of California at San Diego, May 23 1996, M. L. Bushnell.
19. "Redundancy Identification Using Transitive Closure," *Third International Test Synthesis Workshop*, Santa Barbara, CA, May 1996, Q. Lin*, M. L. Bushnell, and V. D. Agrawal.
20. "Built-In and External Test of Known Good Die for Mixed Signal Modules," *ARPA Electronic Packaging and Interconnects Review*, Advanced Research Projects Agency, U.S. Dept. of Defense, Herndon, Virginia, April 1 1996, M. L. Bushnell.
21. "Built-In Delay Testing in Ultra Large Scale Microprocessors," AT&T Bell Laboratories, Murray Hill, New Jersey (teleconferenced to Princeton, NJ), May 25 1995, M. L. Bushnell, I. P. Shaik*, and J. Sienicki*.
22. "Classification and Test Generation for Path-Delay Faults via Single Stuck-Fault Test Generation," *Second International Test Synthesis Workshop*, Santa Barbara, CA, May 1995, M. A. Gharaybeh*, M. L. Bushnell, and V. D. Agrawal.
23. "Sequential Circuit Automatic Test-Pattern Generation," *Semiconductor Research Corporation Multi-University Review*, University of Illinois, Champaign, Illinois, May 18 1995 M. L. Bushnell.
24. "Built-In Delay Testing in Ultra Large Scale Microprocessors," Indian Institute of Technology, Kanpur, India, Jan. 11 1995, M. L. Bushnell.

25. "Built-In Delay Testing in Ultra Large Scale Microprocessors," Indian Institute of Technology, New Delhi, India, Jan. 9 1995, M. L. Bushnell.
26. "Built-In Delay Testing in Ultra Large Scale Microprocessors," North Carolina State U., Raleigh, NC, Electrical Engineering Dept. Seminar, Dec. 17 1994, M. L. Bushnell.
27. "Applications of Discrete Mathematics to Built-In Self-Testing for Delay in Ultra Large Scale Integrated Circuits," *Combinatorics and Optimization in VLSI Design*, RUTCOR, Rutgers U., Piscataway, NJ, Dec. 4 1994, M. L. Bushnell.
28. "Built-In Delay Testing in Ultra Large Scale Microprocessors," Duke U., Durham, NC, Electrical Engineering Dept. Seminar, Nov. 30 1994, M. L. Bushnell.
29. "Decision heuristics for Accelerated Test Generation using Hopfield Neural Nets," *The Joint Conference on Information Sciences*, invited paper, Pinehurst, North Carolina, Nov. 19 1994, M. L. Bushnell and Q. Lin*.
30. "Automatic Test Generation Using Neural Models for Logic Gates and Transistors," Duke University, Durham, NC, VLSI CAD Research Group Seminar, Oct. 28 1994, M. L. Bushnell.
31. "Rapid Application-Specific Electronic Module Design and Test," *Advanced Research Projects Agency Application-Specific Electronic Modules Conference*, IBM, Poughkeepsie, New York, Oct. 1 1994, M. L. Bushnell.
32. "A Graphical Approach to Circuit Cut-Point Placement for Design for Testability," invited paper, *1994 Mathematical Programming Symposium*, University of Michigan, Ann Arbor, Aug. 1994, I. P. Shaik* and M. L. Bushnell.
33. "Mixed Switch & Logic Level Automatic Test Pattern Generation," invited paper, *The Institute of Management Science/Operations Research Society of America*, Anchorage, Alaska, June 12-15 1994, M. L. Bushnell and C. L. C. Cooper*.
34. "Advanced Algorithms for Test-Pattern Generation," *Semiconductor Research Corporation Multi-University Review*, University of Illinois, Champaign, Illinois, May 17 1994, M. L. Bushnell.
35. "Dynamic State and Objective Learning for Sequential Automatic Test-Pattern Generation," AT&T Bell Laboratories Engineering Research Center, Princeton, NJ, Feb. 23 1994, X. Chen* and M. L. Bushnell.
36. "A Robust Delay Fault Model for Built-In Self Testing," University of Southern California, Los Angeles, CA, Feb. 18 1994, M. L. Bushnell.
37. "Rapid Application-Specific Electronic Module Design and Test," *Advanced Research Projects Agency Application-Specific Electronic Modules Conference*, Marina Del Ray, CA, Feb. 15 1994, M. L. Bushnell.
38. "Sequential Circuit Automatic Test-Pattern Generation," *Semiconductor Research Corporation Multi-University Review*, University of Illinois, Champaign, Illinois, May 25-26 1993, M. L. Bushnell.
39. "K-Tree Circuit Partitioning," *The Institute of Management Science/Operations Research Society of America Joint National Meeting*, Chicago, IL, Sponsored Paper, May 16 1993, J. Williams* and M. L. Bushnell.

40. "Energy Minimization Solution of VLSI Test Generation," *The Institute of Management Science/Operations Research Society of America Joint National Meeting*, Chicago, IL, Sponsored Paper, May 16 1993, S. T. Chakradhar*, M. L. Bushnell, and V. D. Agrawal.
41. "Rapid Application-Specific Electronic Module Design and Test," *Advanced Research Projects Agency Application-Specific Electronic Modules Conference*, Phoenix, Arizona, March 23-25 1993, M. L. Bushnell.
42. "Automatic Test Pattern Generation for Delay Fault Testing of State Machines," *Seventh Advanced Research Institute on Discrete Applied Mathematics*, Rutgers Center for Operations Research (RUTCOR), Rutgers U., June 4 1992, M. L. Bushnell.
43. "Sequential Circuit Automatic Test-Pattern Generation," *SRC Joint Test Review*, University of Texas, Austin, TX, April 29 1992, M. L. Bushnell.
44. "Neural Net Models and Algorithms for Test-Pattern Generation," Massachusetts Institute of Technology, Oct. 17 1991, M. L. Bushnell.
45. "Sequential Circuit Automatic Test-Pattern Generation," *SRC Joint Test Review*, University of Illinois, Champaign, Illinois, May 17 1991, M. L. Bushnell.
46. "The New Frontier in Automatic Test-Pattern Generation," AT&T Bell Laboratories Engineering Research Center, Princeton, NJ, Jan. 25 1991, M. L. Bushnell.
47. "Automatic Test-Pattern Generation Using Neural Networks," Siemens Corporation, Princeton Research Lab., Princeton, NJ, Jan. 29 1990, M. L. Bushnell.
48. "New Frontiers in Test-Pattern Generation," McGill University, Montreal, Canada, Nov. 24 1989, M. L. Bushnell.
49. "New Frontiers in Test-Pattern Generation," General Electric Company, Corporate Research and Development Lab., Schenectady, NY, Nov. 1989, M. L. Bushnell.
50. "The New Frontier in Automatic Test-Pattern Generation," IBM Corporation, Poughkeepsie, NY, Oct. 26 1989, J. Giralddi* and M. L. Bushnell.
51. "Massively Accelerated Test-Pattern Generation," Bell Laboratories, Allentown, PA, July 18 1989, M. L. Bushnell.
52. "VLSI CAD Tool Integration Using the Ulysses Design Environment," Siemens Corporation, Princeton Research Lab., Princeton, NJ, June 16 1989, M. L. Bushnell.
53. "Towards Massively Parallel Test-Pattern Generation," Digital Equipment Corporation, DEC Research, Hudson, Mass., April 12 1989, M. L. Bushnell.
54. "Parallel ATPG Algorithms," IBM Corporation, Poughkeepsie, NY, Feb. 20 1989, J. Giralddi* and M. L. Bushnell.
55. "Towards Massively Parallel Test-Pattern Generation," Bell Laboratories, Murray Hill, NJ, Jan. 27 1989, M. L. Bushnell.
56. "VLSI CAD Tool Integration Using the Ulysses Environment," Bell Laboratories, Murray Hill, N. J., Jan. 6 1989, M. L. Bushnell.

57. "Towards Massively Parallel Test-Pattern Generation," Princeton University, Dec. 7 1988, M. L. Bushnell.
58. "Tutorial Paper on Programming Languages," the Instrument Society of America, *Gordon Conference*, Geneva, New York, July 1980, M. L. Bushnell and D. H. Howling.

Panel Activities

1. "Research in Internet Time: How Can We Meet the Challenge?" M. L. Bushnell, *Annual Review, Center for Advanced Information Processing*, Piscataway, NJ, Nov. 15, 2000.
2. "Testing of Low Power Circuits and Systems: Is There Any Need for Special Considerations?," M. L. Bushnell, *Fifth Asian Test Symposium (ATS '96)*, Hsinchu, Taiwan, Nov. 20-22, 1996
3. "Effectiveness of Built-In Self-Testing in Consumer Products," M. L. Bushnell, the *1993 Asian Test Symposium*, Nov. 16-18, 1993, Beijing, China
4. "Applications Using Parallel/Distributed Computing," M. L. Bushnell, the CAIP Center *Parallel/Distributed Computing '92 Symposium*, March 24, 1992

Research Grants M. L. Bushnell is the sole Principal Investigator on all of the following grants, except where otherwise noted.

1. "Test Point Insertion Project," reserach grant, Nippon Electric Company, \$ 12,000, 9/1/2006 - 8/31/2007, M. L. Bushnell, Principal Investigator.
2. "Fault-Tolerant Wireless Networks for Patient Care in the Intensive Care Unit," research grant, Rutgers University Academic Excellence Fund, \$ 50,000, 7/1/2006 - 6/30/2007, M. L. Bushnell, M. Parashar, W. Trappe, Y. Zhang, I. Marsic, Principal Investigators.
3. "NeTs-ProWin: High Performance Cognitive Radio Platform with Integrated Physical and Network Layer Capabilities," research grant # 0435370, National Science Foundation, \$ 1,200,000, 9/1/2004-8/31/2007, D. Raychaudhuri, M. L. Bushnell, R. Yates, N. Mandayam, W. Trappe, R. Frenkiel, I. Seskar, C. Rose, and B. Ackland, Principal Investigators.
4. "Spectral Built-In Self-Testing for Mixed-Signal Systems-in-a-Package (SIP)," research grant # 0429743, National Science Foundation, \$ 300,000, 9/1/2004-8/31/2007, M. L. Bushnell and V. D. Agrawal, Principal Investigators.
5. "System Fault-Tolerance and Testing Models for Nanotechnology," research grant # 2003-RJ-1159G, Semiconductor Research Corporation, Jan., 2004, \$ 40,000, M. L. Bushnell, Principal Investigator.
6. Supplement to "Low-Power System-on-a-Chip Design for Minimum Transient Energy," research grant # 0331813, National Science Foundation, 9/1/20003-6/30/2004, \$ 25,191, M. L. Bushnell and V. D. Agrawal, Principal Investigators.
7. "Digital Spectral Analysis for Mixed-Signal System-on-a-Chip Testing and Verification," research grant # 0098304, National Science Foundation, 4/01/2001-3/31/2004, \$ 513,522, M. L. Bushnell, V. D. Agrawal, and M. Hsiao Principal Investigators.

8. "Low-Power System-on-a-Chip Design for Minimum Transient Energy," research grant # 9988239, National Science Foundation, 9/1/2000-8/31/2003, \$ 131,776, M. L. Bushnell, Principal Investigator.
9. "Analog Data Converter Built-In Self-Testing," research grant, Texas Instruments, 1/1/2000-12/31/2000, \$ 20,000, M. L. Bushnell, Principal Investigator.
10. "Center for Embedded System-on-a-Chip Design," research grant # 99-2042-007-19, New Jersey Commission on Science and Technology, \$ 1,500,000 funded so far, 9/1/99 – 8/31/2004, joint center with Princeton U. and New Jersey Institute of Technology, involving Prof. Bushnell and Caggiano of Rutgers U., 5 Princeton Professors, 1 NJIT Professor, and 1 Virginia Tech. Professor.
11. "Sequential Circuit False Timing Path Identification," research grant, Lucent Technologies, 6/1/98 – 12/31/98, \$ 9,000.
12. "Rapid Logic Circuit Synthesis and Synthesis-for-Testability," research grant, CAIP Research Center, Rutgers University, July 1, 1998 – June 30, 1999, \$ 20,000.
13. "Rutgers Univ./Lucent Technologies Path Delay Fault Program," research grant, Lucent Technologies, 1/1/98 – 2/28/99, \$ 33,071.
14. "Rapid Logic Circuit Synthesis and Synthesis-for-Testability," research grant, CAIP Research Center, Rutgers University, July 1, 1997 – June 30, 1998, \$ 20,000.
15. "Rutgers Univ./Lucent Technologies Path Delay Fault Program," research grant, Lucent Technologies, 2/15/97 – 2/14/98, \$ 33,071.
16. "Automatic Cell Library Technology Migration and Timing Optimization," fee-for-service grant, Mentor Graphics Corp., 2/15/97 – 2/14/98, \$ 23,192.
17. "Rapid Logic Circuit Synthesis and Synthesis-for-Testability," research grant, CAIP Research Center, Rutgers University, July 1, 1996 – June 30, 1997, \$ 24,411.
18. "Built-In and External Test of Known Good Die for Mixed Signal Modules," research grant # F33615-96-1-5610, Advanced Research Projects Agency, U.S. Department of Defense, Application Specific Electronic Modules Program, Jan. 1996 – Dec. 1997, \$ 625,000.
19. "Advanced Algorithms for Test-Pattern Generation," research grant, Semiconductor Research Corporation, Sept. 1995 – Aug. 1996, \$ 73,100.
20. "Automatic Test Vector Generation on Parallel Computers," research grant, CAIP Research Center, Rutgers University, July 1, 1995 – June 30, 1996, \$ 50,000.
21. "Conference Travel Award" for Jim Sienicki, \$ 300 to attend the *8th International Conference on VLSI Design*, New Delhi, India, Jan. 1995.
22. "Advanced Algorithms for Test-Pattern Generation," research grant, Semiconductor Research Corporation, Sept. 1994 – Aug. 1995, \$ 78,000.
23. "Automatic Test Vector Generation on Parallel Computers," research grant, CAIP Research Center, Rutgers University, July 1, 1994 – June 30, 1995, \$ 50,000.

24. "Advanced Algorithms for Test-Pattern Generation," research grant, Semiconductor Research Corporation, Sept. 1993 – Aug. 1994, \$ 87,800, including a competitively won SRC Fellowship for Carolina Cooper and an annual grant of \$ 2,000 to the Rutgers ECE Dept.
25. "Rapid Application-Specific Electronic Module Design and Test," research grant # F33615-93-C-4309, Advanced Research Projects Agency, U.S. Department of Defense, Application Specific Electronic Modules Program, July 1993 – Dec. 1995, \$ 749,769
26. "Automatic Test Vector Generation on Parallel Computers," research grant, CAIP Research Center, Rutgers University, July 1, 1993 – June 30, 1994, \$ 40,000.
27. "Automatic Test Vector Generation on Parallel Computers," research grant, CAIP Research Center, Rutgers University, July 1, 1992 – June 30, 1993, \$ 64,315.
28. "Sequential Circuit Automatic Test-Pattern Generation," research grant, Semiconductor Research Corporation, Sept. 1992 – Aug. 1993, \$ 50,000.
29. "Automatic Test Vector Generation on Parallel Computers," research grant, CAIP Research Center, Rutgers University, July 1, 1991 – June 30, 1992, \$ 68,673.
30. "Trustee's Research Fellowship for Distinguished Young Scholars," 1992, Rutgers University, \$ 3,000.
31. "Sequential Circuit Automatic Test-Pattern Generation," research grant, Semiconductor Research Corporation, Sept. 1991 – Aug. 1992, \$ 50,000.
32. "Donation of a Texas Instruments Explorer-2 19 inch Graphics Work Station" (10 Megabytes of memory, 280 Megabytes of disk storage), research grant, Texas Instruments, March, 1991, valued at \$ 16,008.
33. "Donation of a Hewlett-Packard/Apollo DN4000 Color 19 inch Graphics Work Station" (16 Megabytes of memory, 400 Megabytes of disk storage), research grant, Siemens Corporation, Jan. 1, 1991, valued at \$ 5,500.
34. "Presidential Young Investigator Award," research award, National Science Foundation, Aug. 13, 1990 – Jan. 1, 1996, \$ 125,000, with dollar-for-dollar matching of \$ 187,500 of additional government/industry contributions to the investigator. The total award will be \$ 500,000.
35. "Computer time on the Connection Machine-2," research grant, Northeast Parallel Architectures Center, Nov. 1, 1990 – Nov. 1, 1991.
36. "ULYSSES Design Methodology Project," research grant, CAIP Research Center, Rutgers University, July 1, 1990 – June 30, 1991, \$41,204.
37. "Automatic Test Vector Generation on Parallel Computers," research grant, CAIP Research Center, Rutgers University, July 1, 1990 – June 30, 1991, \$ 65,239.
38. "ULYSSES Design Methodology Project," research grant, CAIP Research Center, Rutgers University, July 1, 1989 – June 30, 1990, \$30,000.
39. "Sequential Circuit Automatic Test-Pattern Generation," research grant, Semiconductor Research Corporation, Sept. 1989 – Aug. 1991, \$ 50,000, with additional matching funds of \$ 50,000.

40. "Automatic Test Vector Generation on Parallel Computers," research grant, CAIP Research Center, Rutgers University, July 1, 1989 – June 30, 1990, \$ 72,637.
41. "SIGDA Travel Grant," travel grant to attend ICCAD '88, Special Interest Group in Design Automation, ACM, Nov. 1988, \$ 1,800.
42. "Young Faculty Grant," research grant, General Electric Foundation, Jan. 1, 1989 – Dec. 31, 1991, \$ 60,000.
43. "SIGDA Travel Grant," travel grant, Special Interest Group in Design Automation, ACM, June 1988, \$ 800.
44. "Automatic Test Vector Generation on Parallel Computers," research grant, CAIP Research Center, Rutgers University, July 1, 1988 – June 30, 1989, \$52,000.
45. "ULYSSES Design Methodology Project," research grant, CAIP Research Center, Rutgers University, July 1, 1987 – June 30, 1988, \$16,000.
46. Henry Rutgers Research Fellowship, research grant, Rutgers University, July 1, 1986 - June 30, 1988, \$30,000.
47. Equipment donation for the American Electronics Association Faculty Development Award, Hewlett-Packard Company, June, 1987, \$ 50,000.

Educational Grants

1. "Donation of 20 Copies of the Cadence Mixed-Signal Chip Layout System" to the Rutgers Foundation, Cadence Design Systems, Inc., Sept. 2001, valued at \$ 3,870,894.
2. "Donation of 50 Copies of the Synopsys Logic Synthesis System" to the Rutgers Foundation, Synopsys, Inc., Sept. 2001, valued at \$ 50,000,000 (\$ 1,000,000 a copy).
3. "Donation of 20 Copies of the Synopsys Logic Synthesis System," Synopsys, Inc., July. 1995, valued at \$ 5,590,800 (\$ 279,540 a copy). This was the largest gift ever received by the Rutgers foundation.
4. "Donation of 10 Copies of the Version 8.2 CAD Tools," Mentor Graphics Corporation, July. 1993.
5. "Donation of 10 Copies of the VHDL Hardware Description Language Software," Mentor Graphics Corporation, Feb. 1993.
6. "Donation of Four Logic Analyzers," Hewlett-Packard Company, Feb. 1993, \$ 29,125.
7. "Grant to Have Educational VLSI Chips Made," NSF, May 1993, \$ 12,000.
8. "Grant to Have Educational VLSI Chips Made," Rutgers University, Feb. 1993, \$ 5,000.
9. "Special Purpose Grant – CAD Work Station and Field-Programmable Gate Array Design Software," AT&T Foundation, Nov. 1992, \$ 15,000.
10. "Donation of Three Additional Copies of the Mentor Graphics Generator Development Tool," Mentor Graphics Corporation, Sept. 1991, valued at \$ 88,000 a copy for a total of \$ 264,000.

11. "Donation of Seven Copies of the Mentor Graphics Generator Development Tool" (produced by the Silicon Compiler Systems Division), Mentor Graphics Corporation, Sept. 1990, valued at \$ 88,000 a copy for a total of \$ 616,000.

Patents

1. *An Area Efficient Mixed-Signal Test Architecture for Systems-on-a-Chip*, U. S. Provisional Patent, Filed Jan. 1, 2006, H. Venkatanarayanan* and M. L. Bushnell.
2. *Graphical IDDQ Signatures for ULSI Testing*, U. S. Patent # 6,812,724 B2, Filed Sept. 11, 2003, Issued Nov. 2, 2004, L. Rao* and M. L. Bushnell.
3. *Graphical IDDQ Signatures for ULSI Testing*, International Patent Application # PCT/US03/05582, International Publication # WO 03/073114 A1, Pending, Filed Sept. 11, 2003, L. Rao* and M. L. Bushnell.
4. *Test Generation for Analog Circuits Using Partitioning and Inverted System Simulation*, U. S. Patent # 6,308,300 B1, Filed June, 1999, Issued Oct. 23, 2001, R. Ramadoss* and M. L. Bushnell.
5. *Method and Apparatus for Combined Stuck-at Fault and Partial-Scanned Delay-fault Built-In Self-Test*, U. S. Patent # 6,247,154 B1, Filed March 1999, Issued Jun. 12, 2001, M. L. Bushnell and G. Parthasarathy*.
6. *Method and System for Identifying Tested Path Delay Faults*, U. S. Patent #6,131,181, Filed Oct. 23, 1997, Issued Oct. 10, 2000, M. A. Gharaybeh*, M. L. Bushnell, and V. D. Agrawal.
7. *Robust Delay Fault Built-In Self-Testing Method and Apparatus, Verfahren und Vorrichtung zur Robusten und Automatischen Prüfung von Verzögerungsfehlern, Procède et Appareil de Test Automatique Intègre D'Anomalie de Retard Dans un Matériel*, European Patent # EP 0 663 092 B1, Filed 7/21/1994, Issued March 22, 2000, M. L. Bushnell and I. Shaik*.
8. *Test Generation for Mixed-Signal Devices Using Signal Flow Graphs*, U.S. Patent # 5,831,437, Filed Jan. 5, 1996, Issued Nov. 3, 1998, R. Ramadoss* and M. L. Bushnell.
9. *Robust Delay Fault Built-In Self-Testing Method and Apparatus*, U.S. Patent # 5,422,891, financed by CAIP Research Center funds, Filed July 23, 1993, Issued June 6, 1995, M. L. Bushnell and I. P. Shaik*.

Fellowships

1. *Board of Trustees Research Fellowship for Distinguished Young Scholars*, Rutgers University, July 1992 – July 1995, \$ 3,000.
2. *Henry Rutgers Research Fellowship*, Rutgers University, Sept. 1986 – Aug. 1988, \$ 30,000 and a reduced teaching load.

Memberships on Editorial Boards

- Member of the Editorial Board of the *Journal of Electronic Testing (Theory and Applications)* published by Kluwer Academic Publishers, for the years 1994-present.
- Member of the Editorial Board of the *International Journal on Artificial Intelligence Tools* published by World Scientific Publishers, for the year 1993. Associate editor for the areas *Artificial Intelligence Tools for VLSI Design* and *Neural Networks*.

Education

- Special honors courses.
 1. *Special Problems Course – Testing of ULSI Circuits*, Summer 1998 Attendees: Scott Birken, Iliyas Pathan
 2. *Special Problems Course – Analog Circuit Simulation*, Summer 1997 Attendees: Phillip Stanley-Marbell, Rajesh Ramadoss, Madhu Iyer, Ganapathy Parthasarathy, Manish Vachharajani, John Sisto, Carlos Parodi

- Undergraduate and Graduate Student Independent Study Supervision

Year	Name	Nature	Title
2006	James Rosado	Research	Baseband Communications Proc. Validation
2006	Wen Yueh	Research	To Be Determined
2005	Suresh Devanathan	Research	Spectral VLSI Testing
2001	Jeff Dwoskin	Research	VLSI Testing
2001	Rajeev Rao	Research	Low-Power Design
2001	Jeff Nelson	Research	BIST Hardware Pattern Generator
2001	Naeem Rehman	Research	EDIF HDL Translator and Data Base
1998	Scott Birken	Research	Sequential Auto. Test-Pattern Gen.
1998	Iliyas Pathan	Research	BIST Machine Embedding into Circuits
1997	John Sisto	Research	Sequential Auto. Test-Pattern Gen.
1997	Manish Vachharajani	Research	Sinc Waveform Analog Circuit Testing
1997	Phillip Stanley-Marbell	Research	Combinational Auto. Test-Pattern Gen.
1996	Xioning Qi	Development	Automatic Test Equipment Interfacing
1996	Carlos Parodi	Development	Logic Schematic Placement and Routing
1996	David Lieber	Development	Logic Schematic Placement and Routing
1996	Prakash Chintamaneni	Research	Automatic Chip Layout Retiming
1995	Steven Crosby	Research	Electromagnetic Product Design and Test
1994	Amit Chhabra	Research	Slade Scholar – Mixed Level Fault Simulation
1994	Allen Dietz	Research	Slade Scholar – Mixed Level Fault Simulation
1993	Ramakrishnan Ganesh	Research	Automatic Test Gen. on a Parallel Computer
1993	Sameer Kalucha	Development	Algorithms and Data Structures for VLSI CAD
1992	Peter Chen	Development	Coding of Sequential Circuit Fault Simulator
1991	Alex Anesko	Development	CAD Tool Coding
1990	Kevin Farrell	Development	CAD Tool Coding
1990	Daehyun Lee	Development	Coding of CAD Tool to Lay Out Chip Pads
1986	Lauraine Schalk	Development	CAD Tool Coding
1986	Tom Vanderwater	Development	CAD Tool Coding

- Postdoctoral Trainees

1. Xinghao Chen – 3 yrs.
 2. Srinivas Mandyam-Komar – 3 2/3 yrs.
- Academic Advisement: Prof. Bushnell advised one quarter of the ECE Dept. senior class from 1991-2000 on academic matters (the number is typically 50 students, but varies).
 - Curriculum Development
 - M. L. Bushnell and V. D. Agrawal have written an undergraduate senior-level textbook entitled *Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits*, which has become the textbook for a model graduate circuit testing course taught at more than 25 leading universities.
 - Instructional Development
 1. First to introduce the teaching of the C Programming Language into Rutgers University. Created 14:332:252 *Programming Methodology I*, the first required programming and data structures course at Rutgers to use C. Students completed 12 demanding programming assignments.
 2. First to introduce the teaching of the VHDL and Verilog Hardware Description Languages into Rutgers University.
 3. Member of the ECE Department Undergraduate Curriculum Committee 1986 – 1995
 4. Created a new Teaching Laboratory for VLSI Computer-Aided Design of integrated circuits with seven color work stations and color plotters.
 5. Participated on the School of Engineering Ad Hoc Committee on Freshman Computing
 6. Introduced *PSpice* simulation into all laboratory assignments in 332:368 *Digital Electronics Lab*.
 7. Bushnell developed the *Automated Teaching Assistant* Program, which was very successfully used at Rutgers for several semesters to teach 180 students Data Structures and C Programming in the sophomore course 332:252 (*Programming Methodology I*). The program cycles through C programs, which are electronically turned in by students, and automatically compiles, links, and executes each program on test data. A TA is shown the program output on a computer screen, and then the program scrolls through the student's source code. After the TA assigns a grade, the program keeps each student's grades in a secure, encrypted, on-line data base, which students can access across the network.

Service

Contributions to the Advancement of the Academic Profession

- Memberships on Editorial Boards
 1. Member of the Editorial Board of the *Journal of Electronic Testing: Theory and Applications* published by Kluwer Academic Publishers, for the years 1994 - Present.
 2. Member of the Editorial Board of the *International Journal on Artificial Intelligence Tools* published by World Scientific Publishers, for the year 1993. Associate editor for the areas *Artificial Intelligence Tools for VLSI Design* and *Neural Networks*.

- Conference Organization and Chairing

1. Program Co-Chairman for *The 19th International Conference on VLSI Design (VLSI Design 2006)*, Jan., 2006 Hyderabad, India.
2. Conference Steering Committee Member for *The North Atlantic Test Workshop – 2005* to present.
3. Conference Finance Co-Chairman for *The North Atlantic Test Workshop (NATW 2004 and NATW 2005)*, May, 2004 and May, 2005 Essex, Vermont.
4. Conference Vice-Chairman for *The North Atlantic Test Workshop (NATW 2003)*, May, 2003 Montauk, New York.
5. Conference Vice-Chairman for *The North Atlantic Test Workshop (NATW 2002)*, May, 2002 Montauk, New York.
6. Program Co-Chairman for *The 9th International Conference on VLSI Design (VLSI Design '96)*, Jan., 1996 Bangalore, India.
7. Program Co-Chairman for *The 8th International Conference on VLSI Design (VLSI Design '95)*, Jan., 1995 New Delhi, India.
8. Awards Committee Member, *14th Int'l. Conf. on VLSI Design (VLSI Design '01)*, Bangalore, India, Jan., 2001.
9. Program Committee Member, *Int'l. Conf. on VLSI Design (VLSI Design)*, India, Jan., 1993-2001.
10. Awards Committee Chairman, *11th Int'l. Conf. on VLSI Design (VLSI Design '98)*, Chennai, India, Jan., 1998.
11. Session Chairman, *Reliable System Test* session, *10th North Atlantic Test Workshop*, May, 2001.
12. Session Chairman, *Test and Design for Testability* session, *10th Int'l. Conf. on VLSI Design (VLSI Design '97)*, Hyderabad, India, Jan., 1997.
13. Session Chairman, *Concurrent Error Detection & Fault Tolerance* session, *Fifth Asian Test Symposium (ATS '96)*, Nov. 20-22, 1996, Hsinchu, Taiwan.
14. Program Committee Member, *EDAC-ETC-EUROASIC Conference*, 1995, Paris, France.
15. Judge, National Poster Session Competition for the Fellows of the Semiconductor Research Corporation, Research Triangle Park, NC, Nov. 21, 1994.
16. Program Committee Member, *Third Asian Test Symposium*, Nov., 1994, Nara, Japan.
17. Session Chairman, *6th Int'l. Conf. on VLSI Design (VLSI Design '93)*, Jan., 1993 Bombay, India., *Testing* session.
18. Session Chairman, *New Modeling and Test Techniques* session, *5th Int'l. Conf. on VLSI Design (VLSI Design '92)*, Jan. 4-7, 1992, Bangalore, India.

- Government, Journal and Conference Reviewing

1. Reviewer, *National Science Foundation* of the United States
2. Reviewer, *IEEE Trans. on Computer-Aided Design* Journal
3. Reviewer, *IEEE Trans. on VLSI Systems* Journal
4. Reviewer, *Proceedings of the IEEE* Journal

5. Reviewer, *IEEE Trans. on Computers Journal*
 6. Reviewer, *IEEE Trans. on Systems, Man, and Cybernetics Journal*
 7. Reviewer, *IEEE Trans. on Parallel and Distributed Systems Journal*
 8. Reviewer, *IEEE Computer Magazine Journal*
 9. Reviewer, *IEEE International Test Conference*
 10. Reviewer, *IEEE Annual International Symposium on Fault-Tolerant Computing*
 11. Reviewer, *International Conference on VLSI Design*
 12. Reviewer, *IEEE VLSI Test Symposium*
 13. Reviewer, *IEEE International Symposium on Circuits and Systems*
 14. Reviewer, *ACM/IEEE Design Automation Conference*
 15. Reviewer, *IEEE International Workshop on Electronics Design, Test & Applications*
- Society Memberships
 1. Senior Member of the IEEE – Computer Society, Circuits and Systems Society, Communications Society, Engineering Management Society.
 2. Member of the ACM – Special Interest Groups for Design Automation, Artificial Intelligence
 3. Member of the VLSI Society of India (VSI)

University Service

- Member, CAIP Future Direction and Leadership Committee, 2004-2005
- Elected Graduate Director, Dept. of Electrical and Computer Engineering, Rutgers U., 9/1/99 - 6/30/2003
- Elected Member, Rutgers University Senate, representing the School of Engineering, 1998-2003
- Member, New Brunswick Computing Advisory Committee, 1998-1999.
- Member, New Brunswick Information Sciences Council, 1998-1999.
- Member, New Brunswick Transportation Coordinating Council, 1998-1999.
- Member, Provost's Committee for the Cluster Review of Computer Research and Education, 1996
- Member, Graduate School New Brunswick Disciplinary Committee

Contributions to the Rutgers School of Engineering

1. Member, ECE Department Qualifying Examination Committee, 1992 – Present
2. Member, ECE Department Admissions Committee, 1992 – Present
3. Member, School of Engineering Committee on Committees, 1997 – 1999

4. Member of the School of Engineering Ad Hoc Committee on Freshman Computing
5. Member of the Electrical and Computer Engineering Dept. Undergraduate Curriculum Committee, 1986 – 1995. Participated in development of the initial Computer Engineering Curriculum in the ECE Department at Rutgers University.
6. Member of the Center for Computer Aids for Industrial Productivity Equipment Committee
7. Created a new Research Laboratory for VLSI Computer-Aided Design with nine color work stations, a laser printer, a copier, color plotters, and an automatic test equipment.

Contributions to Society at Large

• Industrial Technology Transfer

1. The following patents were sold to Intellectual Ventures for development:
 - (a) *Test Generation for Analog Circuits Using Partitioning and Inverted System Simulation*, U. S. Patent # 6,308,300 B1, Filed June, 1999, Issued Oct. 23, 2001, R. Ramadoss* and M. L. Bushnell.
 - (b) *Test Generation for Mixed-Signal Devices Using Signal Flow Graphs*, U.S. Patent # 5,831,437, Filed Jan. 5, 1996, Issued Nov. 3, 1998, R. Ramadoss* and M. L. Bushnell. and
 - (c) *Robust Delay Fault Built-In Self-Testing Method and Apparatus*, U.S. Patent # 5,422,891, financed by CAIP Research Center funds, Filed July 23, 1993, Issued June 6, 1995, M. L. Bushnell and I. P. Shaik*.
2. The *Combinational EST* automatic test-pattern generator for combinational circuits, developed by Bushnell and Giraldi*, was licensed to Boolean Dynamics of New York City for development as a formal hardware verification tool.
3. The *Sequential EST* (SEST) automatic test-pattern generator for sequential circuits, developed by Bushnell and Chen*, was licensed to Boolean Dynamics of New York City for development as a formal hardware verification tool.
4. The *Sequential EST* (SEST) automatic test-pattern generator for sequential circuits, developed by Bushnell and Chen*, was adopted as the standard sequential ATPG program in IBM's TESTBENCH tools. SEST was used to design and test IBM's first partial-scan microprocessor with 50 million transistors. 200 copies of TESTBENCH have been sold outside of IBM. **SEST** was also transferred to NEC Corporation (Princeton, NJ), Texas Instruments, Carnegie Mellon U., and the U. of Tennessee.
5. The path delay-fault simulator and false timing path detector developed by Bushnell, Gharaybeh*, and Agrawal was transferred to Lucent Technologies Engineering Research Center in Princeton, New Jersey, and incorporated into the company's standard testing tool suite. The tool is called SPDF and is currently being used at Lucent Microelectronics to test a 623 MHertz state-of-the-art SONET ring communications chip for the company's # 5 ESS Electronic Switching Long-Distance Telephone Exchanges.
6. Bushnell and Chen's* theory of full-custom VLSI layout area estimation has been incorporated into CAD software products provided by Indian Telephone Industries and is widely used at Intel Corp.

7. Bushnell and Brasen's* work on full-custom VLSI chip floorplanning and switchbox routing to reduce timing delay was used by Compass Design Automation in their CAD software products.
8. The **EST** redundant logic eliminator and test-pattern generator program developed by Bushnell and Giraldi* was transferred to IBM at Poughkeepsie, New York, and Texas Instruments at Dallas, Texas.
9. The **NNATPG** neural network-based redundant logic eliminator and test-pattern generator program, developed by Bushnell and Chakradhar* at Rutgers, was enhanced and adopted as the standard corporate test-pattern generator called *TRAN* at the Nippon Electric Company, worldwide.
10. While at the Instron Corporation, Dr. Bushnell was the first person world wide to perform the vital Thermal-Mechanical Fatigue testing for Jet Aircraft Engine turbine blades using a digital computer to control a Materials Testing Instrument. This work led to more accurate characterization of turbine materials in the commercial and military jet engine industry. The computer software and testing equipment developed by Dr. Bushnell were deployed first at *Pratt and Whitney* and later also at *General Electric* and at *Westinghouse*.

PhD Theses Supervised

1. Lan Rao, PhD, Rutgers University, ECE Dept., October, 2003, *Graphical CMOS I_{DDQ} Signatures Based on Data Mining* – Sun Microsystems, Santa Clara, California.
2. Tezaswi Raja, PhD, Rutgers University, ECE Dept., May, 2004, *Minimum Dynamic Power Design of CMOS Circuits Using Variable Input Delay Logic* – Trans-Meta Corp., Santa Clara, California.
3. Marwan Gharaybeh, PhD, Rutgers University, ECE Dept., July, 1996, *On Testing High-Speed Digital VLSI Circuits* – Synopsys, Inc., Mountain View, California.
4. Imtiaz Shaik, PhD, Rutgers University, ECE Dept., June, 1996, *Robust Built-In Self-Testing for Combinational Circuit Delay Faults* – Advanced Micro Devices, Milpitas, California.
5. James Sienicki, PhD, Rutgers University, ECE Dept., October, 1995, *Super-Linear Speedup in Distributed Test Generation Algorithms* – Ariel Corp., Cranbury, NJ.
6. Tapan Chakraborty, PhD, Rutgers University, ECE Dept., October, 1993, *Delay Fault Test-Pattern Generation for Random Logic State Machines* – Lucent Technologies Bell Laboratories Engineering Research Center, Princeton, NJ.
7. Xinghao Chen, PhD, Rutgers University, ECE Dept., October 1993, *State and Objective Learning for Sequential Circuit Automatic Test-Pattern Generation* – IBM Corp., Endicott Junction, New York.
8. John Giraldi, PhD, Rutgers University, ECE Dept., October 1990, *Search Space Equivalence for Combinational Redundancy Identification and Test-Pattern Generation* – IBM Corp., Poughkeepsie, New York.
9. Srimat Chakradhar, PhD, Rutgers University, Computer Science Dept., May 1990, *Neural Network Models for Test-Pattern Generation* – NEC Research Institute, Princeton, NJ.

Current PhD Thesis Supervision

1. Omar Khan, *Statistical Response Compacters and DFT Hardware for Built-In Self-Testing of Sequential Digital Circuits*.
2. Baozhen Yu, *Low-Power Chip Operation Using Dynamic Power Cutoff*.
3. Hari Vijay Venkatanarayanan, *Statistical Testing for Analog Circuits*.
4. Rajamani Sethuram, *Concurrent Implication Graphics for Formal Verification and Testing*

Masters Theses Supervised

1. Jeff Ayres, M.S., Rutgers University ECE Dept., Jan. 2006, *A Tiered Approach to Analog Circuit Testing Using ARMA Models*
2. Rajamani Sethuram, Rutgers Universtiy ECE Dept., Oct. 2005, *Sequential Automatic Test-Pattern Generation Using Concurrent Implications over Time*
3. Dan Mazor, M.S., Rutgers University, ECE Dept., Oct. 2005, *Nanotechnology Single Electron Transistors*.
4. Siri Uppalapati, M.S., Rutgers University, ECE Dept., Oct. 2004, *Low Power Design of Standard Cell Digital VLSI Circuits*.
5. Hari Vijay Venkatanarayanan, M.S., Rutgers University, ECE Dept., Oct. 2004, *An Area Efficient Test Architecture for Mixed-Signal Systems-on-a-Chip*.
6. Kunal Dave, M.S., Rutgers University, ECE Dept., May 2004, *Using Contrapositive Rule to Enhance the Implication Graphs of Logic Circuits*.
7. Shweta Chary, M.S., Rutgers University, ECE Dept., Oct. 2003, *Simulation-Based Test-Pattern Generation for Combined Resistive and Capacitive Coupling Faults*.
8. Karthikeya Parameswaran, M.S., Rutgers University, ECE Dept., Oct. 2003, *A Quasi-Adiabatic Logic ARMCORE Microprocessor*.
9. Omar Khan, M.S., Rutgers University, ECE Dept., Oct. 2003, *Statistical Response Compaction for Built-In Self-Test Systems Using Spectral Techniques*
10. Swathi Jayaramaiah, M.S., Rutgers University, ECE Dept., Oct. 2003, *Analog Circuit Test Generation and Backtracing Using Auto Regressive Moving Average (ARMA) Coefficients*
11. Krishna Upadhyayula, M.S., Rutgers University, ECE Dept., Oct. 2003, *Test Pattern Generation Using Spectral Built-In Self-Test*
12. Junwu Zhang, M.S., Rutgers University, ECE Dept., Oct. 2003, *Improving the Spectrum-Based Sequential ATPG Techniques*
13. Vishal Mehta, M.S., Rutgers University, ECE Dept., May 2003, *Redundancy Identification in Logic Circuits Using Extended Implication Graph and Stem Unobservability Theorems*
14. Sameer Mangalampalli, M.S., Rutgers University, ECE Dept., Jan. 2003, *A Spectral Based Built-In Self-Test Method for Mixed-Signal and Analog Circuits*

15. Tezaswi Raja, M.S., Rutgers University, ECE Dept., May 2002, *A Reduced Constraint Set Linear Program for Low-Power Design of Digital Circuits*
16. Vivek Gaur, M.S., Rutgers University, ECE Dept., Jan. 2002, *A New Transitive Closure Algorithm to Identify Redundancies in Logic Circuits*
17. Aditya Sathe, M.S., Rutgers University, ECE Dept., Jan. 2002, *Non-ATPG Techniques for Testing On-Chip Interconnect Coupling Faults*
18. Abhishek Bisaria, M.S., Rutgers University, ECE Dept., Jan. 2002, *Digital Spectral Test Generation for Mixed-Signal Circuit Testing*
19. Sanjay Mohan, M.S., Rutgers University, ECE Dept., Oct. 2000, *Code Transition Delay Fault Models for A/D Converter Testing*
20. Carlos Parodi, M.S., Rutgers University, ECE Dept., Jan. 1999, *Exact Non-Enumerative Path-Delay Fault Simulation of Sequential Circuits*
21. Madhu Iyer, M.S., Rutgers University, ECE Dept., Jan. 1998, *Effect of Noise on Analog Circuit Testing*
22. Ganapathy Parthasarathy, M.S., Rutgers University, ECE Dept., Jan. 1998, *Delay Fault Built-In Self-Test and Partial-Scan Insertion for Sequential Circuits*
23. Lakshminarayana Pappu, M.S., Rutgers University, ECE Dept., June 1996, *Statistical Path and Gate Delay Fault Coverage Estimation in Sequential Circuits*
24. Pomeli Ghosh, M.S., Rutgers University, ECE Dept., May 1996, *Transistor Stuck-Open Fault Test Generation for Switch-Level Circuits Using Energy Minimization Techniques*
25. Rajesh Ramadoss, M.S., Rutgers University, ECE Dept., February 1996, *Test Generation for Mixed-Signal Devices Using Signal Flow Graphs* (defense held up because a patent was filed on the work).
26. Qing Lin, M.S., Rutgers University, ECE Dept., January 1996, *Efficient Techniques for a Transitive Closure-Based Test Generation Algorithm.*
27. Carolina Cooper, M.S., Rutgers University, ECE Dept., January 1994, *Automatic Switch-Level Test Generation Using Energy Minimization*
28. Keerthinarayan Heragu, M.S., Rutgers University, ECE Dept., May 1994, *Approximate and Statistical Methods to Compute Delay Fault Coverage*
29. Imtiaz Shaik, M.S., Rutgers University, ECE Dept., May 1993, *Robust Built-In Self-Testing for Circuit Delay Faults*
30. James Sienicki, M.S., Rutgers University, ECE Dept., October 1992, *Graphical Methodology Language for CAD Frameworks*
31. Sandip Parikh, M.S., Rutgers University, ECE Dept., October 1992, *Automatic CAD Tool Execution in the Ulysses II CAD Framework*
32. Joseph Williams, M.S., Rutgers University, ECE Dept., October 1992, *K-Tree Circuit Partitioning*

33. Andrew Chang, M.S., Rutgers University, ECE Dept., May 1992, *An Implementation of Constrained Quadratic 0-1 Programming for Automatic Test Pattern Generation for VLSI Circuits*
34. Dan Adler, M.S., Rutgers University, ECE Dept., October 1990, *A Parallel Switch-Level Circuit Simulator*
35. Dan Brasen, M.S., Rutgers University, ECE Dept., October 1989, *Full-Custom Macro Cell Floorplanning and Placement Under Timing Constraints*
36. Xinghao Chen, M.S., Rutgers University, ECE Dept., May 1988, *Full-Custom Layout Area and Aspect Ratio Estimation*

Current Masters Thesis Supervision

1. Lakshmi Balasubramanian, *Low-Power Microprocessor Design*
2. Varadan Veeravalli Savulimedu, *Low-Power Baseband Processor Design*
3. Sharanya Chandrasekar, *Low-Power VLSI Design*
4. Rohit Pandey, *Wireless Baseband Processor Architectures*
5. Gagandeep Sandha, *False Path Detection in Linear Time*

Research in Teaching Computer Engineering

1. We have developed the *Automated Teaching Assistant* Program, which was very successfully used at Rutgers for several semesters to teach 180 students Data Structures and C Programming in the sophomore course 332:252 (*Programming Methodology*). The program cycles through C programs, which are electronically turned in by students, and automatically compiles, links, and executes each program on test data. A TA is shown the program output on a computer screen, and then the program scrolls through the student's source code. After the TA assigns a grade, the program keeps each student's grades in a secure on-line data base, which students can access across the network.