Graduate Course for Spring 2008
TESTING OF
ULTRA LARGE SCALE INTEGRATED CIRCUITS
16:332:576
Section 01

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Jan. 15, 2008

This course covers the testing of *Ultra Large Scale Integrated Circuits* (*ULSI*), the design of circuits for testability, the design of built-in self-testing circuits, and the use of IEEE Boundary Scan Standards. Intel's $0.13\mu m$ feature size Pentium 4 Extreme Edition μprocessor contained 396 million transistors in 2003, ran at 3.2 GHz, and consumed 81.8 W of energy. *Testing* determines whether a manufactured ULSI circuit has broken wires or transistors. *Design for Testability* is necessary, since testing is so difficult that we must explicitly synthesize circuits to be testable and testing must be considered during all design phases. Testing of circuits is one of the most critical obstacles to designing microprocessors and *Application Specific Integrated Circuits* (*ASIC's*). Chip designers, who want to learn about design for testability in order to design better chips, and researchers, who wish to develop algorithms and patents for testing, should take this course. Verification testing and production testing represent 50 to 60 % of the cost of making VLSI chips, and are now the biggest cost of this technology. The course has a series of lectures, and each student must give a twenty minute in-depth lecture on a topic that he/she has researched in the literature. Each student will have to turn in a *well-researched* and *well-written* paper on his topic. The course level is appropriate for a college senior or a first year graduate student with experience in Digital Electronics Design. The course meets once a week, for 3 hours each time. Bushnell and Agrawal have written a testing textbook based on this course, which is now used by most Universities world-wide that teach circuit testing.

PROFESSOR:	Michael L. Bushnell	Room 624, CORE Bldg.
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Bushnell's Email Address:	bushnell@caip.rutgers.edu	
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Course Web site:	http://www.caip.rutgers.edu/∼ bushnell	
Bushnell's Office Hours:	Tues. and Thurs., 1:30-4:30 p.m.	
Meeting Room:	Room 538, CORE Building	
Meeting Time:	Friday, 6:40 - 9:30 p.m.	
First Meeting:	Friday, Jan. 25, 2008	
Course Completion Date:	May 2, 2008	
Course Laboratory:	CORE 601A and CORE 533	

TEXTBOOK:

- *Essentials of Electronic Testing: Digital, Analog, and Mixed-Signal*, Bushnell and Agrawal, Kluwer Academic Press, Boston, 2000, third printing, ISBN # 0-7923-799-1-8.

REFERENCE BOOKS:

- See Appendix C of the Bushnell & Agrawal textbook.

ASSUMED BACKGROUND:

Boolean Algebra
Sequential Circuit Logic Design
C and C++ Language Programming
Elementary MOS Transistor Circuits
Combinational Circuit Logic Design
College Sophomore Electrical Network Theory
RISC Computer Architecture

WORK EXPECTED OF STUDENTS. The course will meet once a week, each meeting for 3 hours, for 13 weeks. There are a series of lectures that each student is expected to attend. Each student will have to complete all of these items:

1. A twenty minute in-depth presentation on a testing topic that he/she has researched in the literature. The student talk must SUPPLEMENT, not REITERATE, material presented by the main lecturer(s). Please prepare powerpoint slides so that your talk goes faster.

2. An individual programming or design project, in which he/she writes part of a Computer-Aided Design program for circuit testing in C++, or develops a testing circuit, or analyzes testing data. The programming project must be demonstrated to the rest of the class at the term end.

3. Thirteen homework assignments on the various test-pattern generation algorithms and on the structure of scan-design and built-in self-testing circuits. Homework (except for the last one) is due exactly 2 weeks after it is assigned.

4. A *well-researched* and *well-written* paper (of at most 6 pages) describing his/her topic, with proper literature citations. Badly written papers will be returned to you for rewriting. For examples on how to correctly write technical papers, look at the papers cited in Bushnell and Agrawal.

5. A final examination.

NEW TEST BOOK EDITION. Prof. Agrawal and I are creating the second edition of the testing book as part of this course. You will be exposed to two new chapters, *Radio Frequency Analog Test* and *Test Data Compression*. Also, all of the homework problems will be new for this course. Expect the course lecture schedule to be adjusted as the course proceeds. Any suggestions from you (both complimentary and critical) about the course and its textbook would be greatly appreciated.

SCHEDULE OF TOPICS:

Topic	Reading Chapter	Slide Show	Dates	Home-work
Part I – Introduction to Testing				
Test Introduction & Test Equipment	1-2	1-2	1/25/08	1
Test Economics, Product Quality, & Fault Modeling	3-4	3-5	2/1/08	2
Part II – Test Methods				
Logic & Fault Simulation	5	6-7	2/8/08	3
Testability Measures and Combinational Automatic Test-Pattern Generation (ATPG)	6-7	8-10	2/15/08	4
Combinational ATPG (Continued)	7	11-12	2/22/08	5
Sequential Automatic Test-Pattern Generation	8	13-14	2/29/08	6
Memory Testing	9	15-16	3/7/08	7
Analog Testing	10-11	17-19	3/14/08	8
Delay Fault and IDDQ Testing	12-13	20-22	3/28/08	9
Part III – Design for Testability				
Design for Testability	14	23-24	4/4/08	10
Built-In Self-Testing I	15	25	4/11/08	11
Built-In Self-Testing II	15	26-27	4/18/08	–
Boundary Scan & Mixed-Signal Test Bus	16-17	28-30	4/25/08	12
System Test & CORE-Based Design	18	31	5/2/08	13

GRADING:

Homeworks 1-13 (Only the 10 best are included)	25 %
20 Min. In-Class Presentation	10 %
Final Paper	15 %
Course Project	30 %
Final Examination	20 %
Total	100 %

Note that if you do not interact with the rest of the class during the term, then your In-Class Presentation grade will be reduced.

HOMEWORK AND FINAL EXAM TOPICS:

1. *Homework 1:* Test Introduction and ATE
2. *Homework 2:* Test Economics and Fault Modeling
3. *Homework 3:* Logic and Fault Simulation
4. *Homework 4:* Testability Measures
5. *Homework 5:* Combinational ATPG
6. *Homework 6:* Sequential ATPG

7. *Homework 7:* Memory Testing
8. *Homework 8:* Analog Testing
9. *Homework 9:* Delay Fault Testing & IDDQ Testing
10. *Homework 10:* Design for Testability
11. *Homework 11:* Built-In Self-Testing
12. *Homework 12:* Boundary Scan and Analog Test Bus
13. *Homework 13:* System Test and CORE-Based Design
14. *Final Exam:* All Topics

HOMEWORK SUBMISSION POLICIES:

1. Homework is due 2 weeks after it is assigned.
2. You may email your homework to *bushnell@caip.rutgers.edu*, provided that your assignment consists of a single pdf file attachment. If you send multiple files that I have to assemble, I will not accept email homework.
3. You may FAX your homework to (732) 445-4775 or you may use slow mail. My address is:

   Prof. Michael L. Bushnell
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4. The time stamp or postmark on your homework sent either by FAX, slow mail, or email must be before Midnight on the day it is due. Otherwise, you will be penalized.
5. Homework solutions will NOT be put up on the course web site or emailed to you, because most universities around the world use our textbook, and the solutions have a history of circulating on the internet.
6. You are expected to work individually with NO COLLABORATION on your homework.