

Spring 2008  
 TESTING OF  
 ULTRA LARGE SCALE INTEGRATED CIRCUITS  
 16:332:576  
 Homework 10  
 Assigned April 4, 2008 – Due April 18, 2008

Reading Assignment: Chapter 14

## 1 Digital DFT and Scan Design

- 14.15 *Illinois scan*. A variant of full-scan called Illinois scan [1, 2] is used to halve the scan chain length and shorten the test application time. The scan chain is divided into two parts of equal length, with the *scan\_in* input to both chains driven by a common pin. For the circuit in Figure 1, with the two sub-scan chains, collapse all of the faults between the flip-flops using the *Checkpoint Theorem*. Then, determine which of those faults are testable using Illinois scan. For the untestable faults, indicate whether the fault is untestable in the functional circuit, or whether the Illinois scan constraint made it untestable.

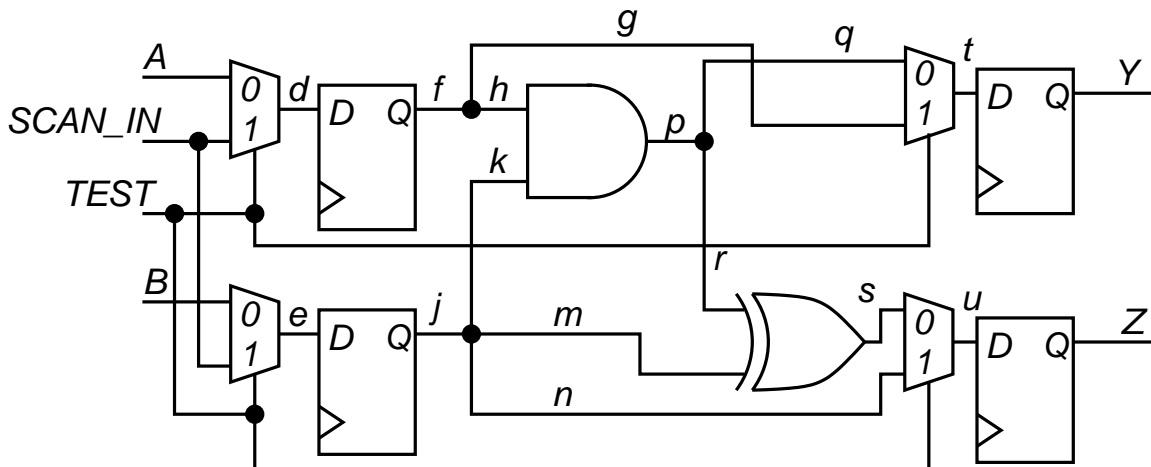


Figure 1: Circuit for Problem 14.15.

- 14.16 *Scan hardware overhead*. For a chip with 20 million logic gates and 50,000 flip-flops, a combinational ATPG program produced  $100 \times 10^6$  test vectors. Find the scan test length if

500 scan chains are implemented. If the circuit has 250 *primary input* (PI) and 200 *primary output* (PO) data pins, and only one extra pin can be added for test, how much more logic gate overhead will be needed for the new design with the DFT hardware?

- 14.17 *Partial-scan*. Consider the circuit *s27* in Figure 2. Draw the s-graph for the circuit and identify the flip-flop(s) to be scanned such that all cycles are broken.

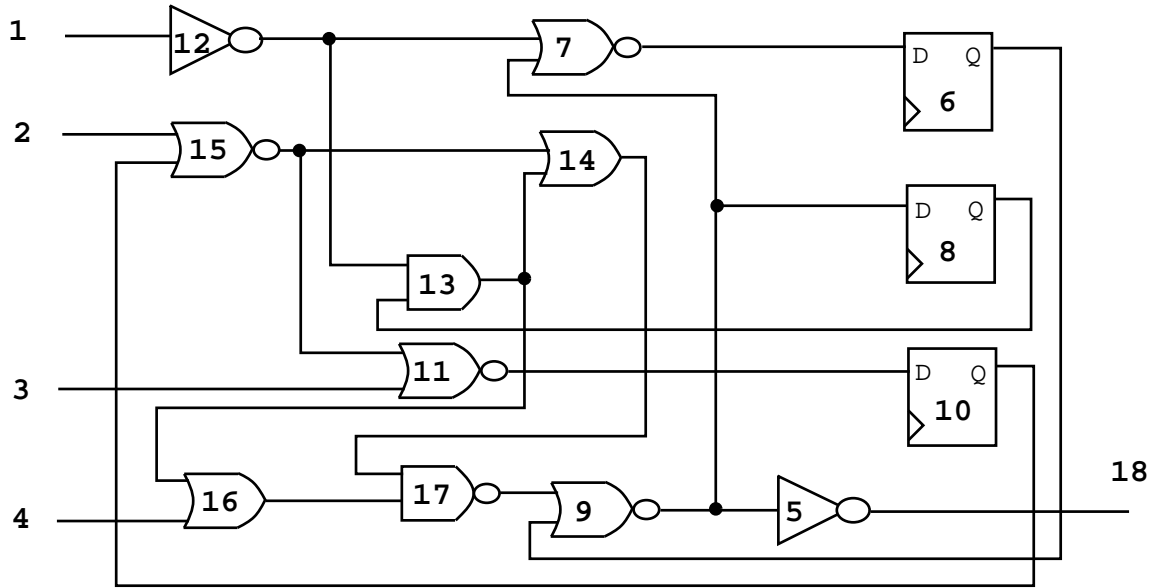


Figure 2: *s27* Circuit for Problem 14.17.

- 14.18 *Sequential ATPG for partial-scan*. Use a sequential ATPG program to generate tests for the circuit of Figure 3. Determine which fault sites are untestable from the ATPG program and scan the flip-flop(s) closest to the untestable fault sites. Rerun the ATPG program. Iterate until you get 100% fault coverage. Report the scan hardware overhead and the number of DFT iterations required to make the circuit testable.
- 14.19 *Scan delay tests*. For the circuit in Figure 4, insert scan-hold flip-flops. Generate robust delay tests for all paths. Then, repeat the exercise in functional sequential mode (with no scan hardware). What is the difference in the outcome between the two cases?

## References

- [1] I. Hamzaoglu and J. H. Patel. Reducing Test Application Time for Full Scan Embedded Cores. In *Proc. of the International Fault-Tolerant Computing Symp.*, pages 260–267, 1999.
- [2] K. J. Lee, J. J. Chen, and C. H. Huang. Using a Single Input to Support Multiple Scan Chains. In *Proc. of the International Conf. on Computer-Aided Design*, pages 74–78, 1998.

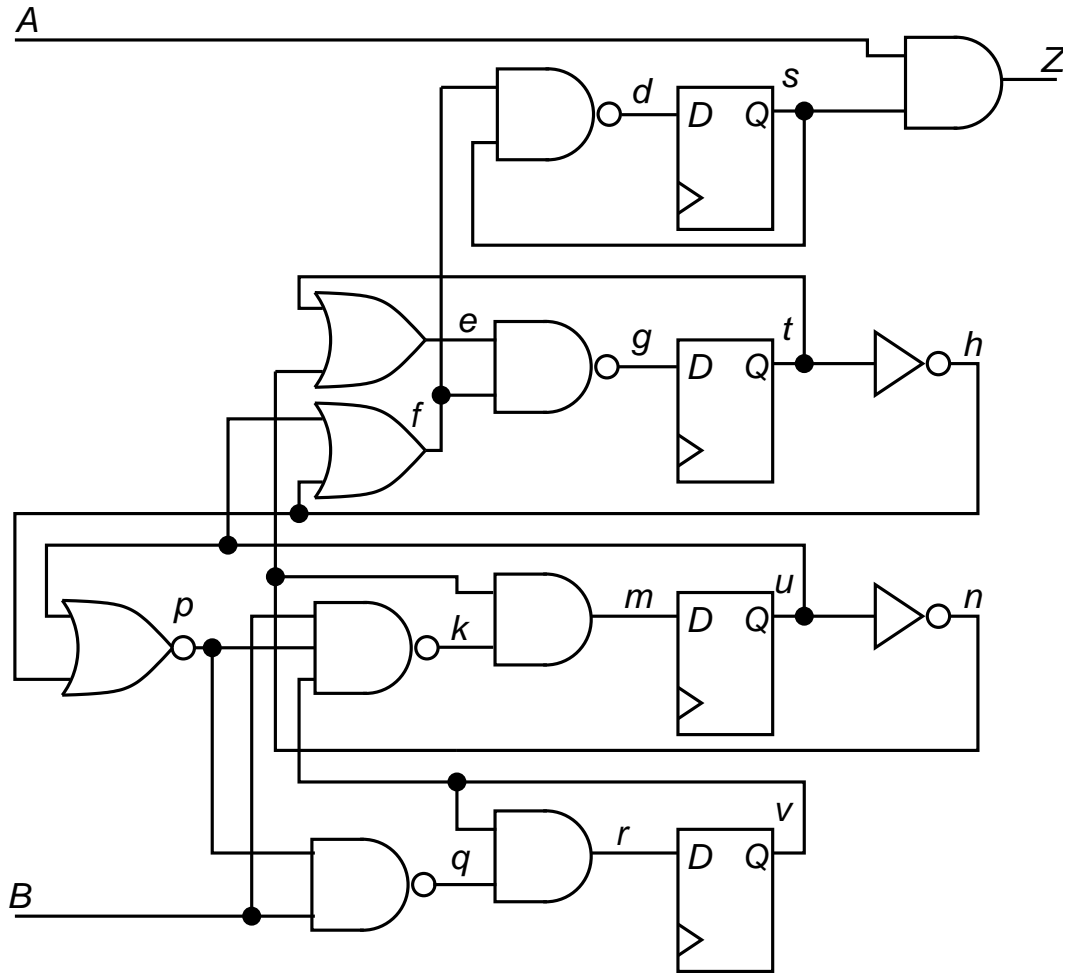


Figure 3: Circuit for Problem 14.18.

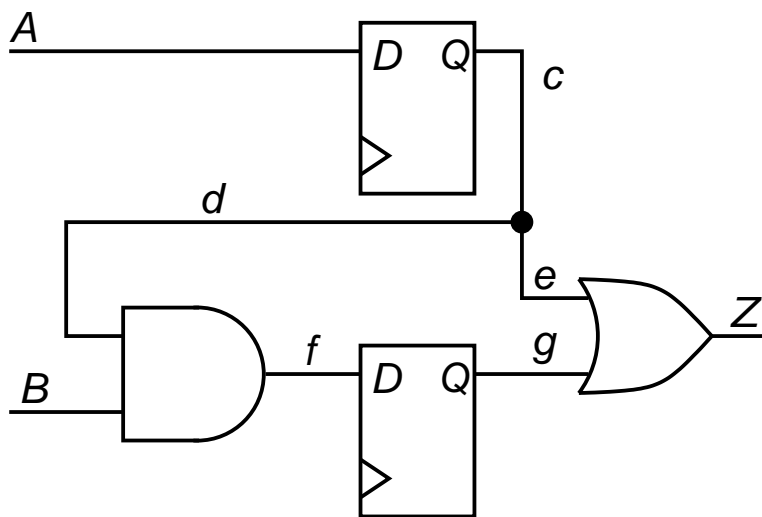


Figure 4: Circuit for Problem 14.19.