

Spring 2008  
 TESTING OF  
 ULTRA LARGE SCALE INTEGRATED CIRCUITS  
 16:332:576  
 Homework 12  
 Assigned April 18, 2008 – Due May 2, 2008

Reading Assignment: Chapters 16 & 17

## 1 Boundary Scan and Analog Test Bus Standards

- 16.11 *Boundary scan DFT.* Repeat Problem 16.1 but add in the hardware overhead for the TAP controller, the ID register, and the Bypass register.
- 16.12 *Boundary scan economics.* Repeat Problem 16.2, but for the case where the chip has 1500 pins and a test clocking rate of 500 *MHz*.
- 16.13 *Boundary scan test time.* The printed circuit board in Figure 16.8 has four chips with these characteristics:

Chip	# Test patterns	# Pins	Chip	# Test patterns	# Pins
Chip1	1,000,000	1,500	Chip3	2,000,000	1,000
Chip2	6,000,000	1,000	Chip4	4,000,000	1,000

Compute the test time for four testing episodes at a test and board clock rate of 512 *MHz*, without using the JTAG BYPASS instruction, to test only Chips 1-4 (and not the interconnect) using an external tester applying the patterns through the JTAG boundary scan chain. Now, recompute the testing time for only Chips 1-4 using the JTAG BYPASS instruction.

## 2 Analog Test Bus

- 17.7 *Chip area overhead.* Assume that each analog switching transistor in the analog test bus hardware has ten times the area of a minimum-sized digital transistor. Estimate the chip area of a digital DBM and a complete ABM as follows:

$$\begin{aligned}
 \text{Area} &= \sum \text{Transistor areas} + \text{Interconnect overhead} \\
 \text{Interconnect overhead} &= 0.4 \times \text{Total transistor area}
 \end{aligned}$$

Calculate the ratio of the ABM area to the DBM area.

17.8 *Transformer test.* Modify the circuit of Figure 17.8 (a) to test the two windings of an external transformer connected to the circuit. The transformer has a turns ratio of 1 : 50. The transformer replaces the  $Z$  component in Figure 17.8(a), except that there are now two  $Z$  components, so you must add additional ABMs. Please propose test waveforms and a series of measurements. Assume that switches  $S5$ ,  $S6$ ,  $SB1$ ,  $SB2$ , and  $SG$  each introduce a  $100\ \Omega$  parasitic resistor when they are on. If the transformer needs to be accurate to 1% and your system voltmeter has  $20\ \mu V$  error in each measurement, does measurement error exceed the transformer tolerance?