

Spring 2008  
TESTING OF  
ULTRA LARGE SCALE INTEGRATED CIRCUITS  
16:332:576  
Homework 1  
Assigned Jan. 25, 2008 – Due Feb. 8, 2008

Reading Assignment: Chapters 1 & 2

## 1 Introduction

- 1.6 *Test cost.* A semiconductor company currently makes micro-controller chips, performs the wafer-sort test on the bare die, packages the chips, and finally performs packaged part test. It is proposed to eliminate the wafer-sort test. The wafer-sort test uses 100,000 vectors and the packaged part test uses 5,000,000 vectors. Both tests operate at 200 *MHz*. Assuming that ATE time costs 4.56 *cents/s*, wafer-sort test yield is 96%, and packaged part yield is 97%, determine whether it makes economic sense to eliminate the wafer-sort test (show an economic analysis). If the chip production volume is 80 *million/year* and the package costs \$ 1.99, determine how much the elimination of wafer-sort test would save or cost over one year.
- 1.7 *Test cost.* Calculate the test cost per chip for a mixed-signal part with 1500 digital pins. It takes 6 *s* of ATE time to perform the analog test, and there are  $1.5 \times 10^9$  digital and memory test vectors, which are applied at the rate of 1 *GHz*. Assuming a yield of 67% and a 1 *GHz* ATE, calculate the test component to be added to the price of a good chip. The ATE has a main frame cost of \$ 1.5 million, and an additional per-pin cost of \$ 4000. Depreciate the ATE linearly over 5 years, assume an annual maintenance cost of 2% of the ATE purchase cost, and assume an annual operating cost of \$ 0.5 million.

## 2 Automatic Test Equipment

- 2.6 *Test ordering.* A chip technology has low yield from AC parametric tests, because of excessive timing faults within the chip. Assume the following test costs and yields:

Test #	Test Type	Cost (cents)	Yield
1.	Wafer sort	11	78%
2.	Contact test	2	96%
3.	Functional test	15	80%
4.	DC parametric test	2	95%
5.	AC parametric test	3	60%

For an annual production of 20 million chips, calculate the most cost-effective order of the tests that leads to the lowest testing cost. How much test money did you save over 1 year?

2.7 *Multi-site testing.* A tester can be equipped to do multi-site testing of 2, 4, or 8 chips at a time instead of just one chip. The pin electronics for the extra pins to be read by the tester must be duplicated. Assume that the chip handler cost is \$ 0.5 million, and doubles each time you double the number of chips for multi-site testing. Include the handler cost in the tester cost calculation. The ATE has a \$ 1.5 million main frame cost, and \$ 2000 for each pin. Assume linear depreciation over 5 years, assume 2% of the ATE purchase price for annual maintenance costs, and assume \$ 0.5 million for annual operating costs. The *device-under-test* (DUT) is digital and has 1,000 pins, of which 250 are output pins. Assume that the tester operates at 10 *MHz* and that the test vector set has 10 million vectors. Calculate the cost of adding chip # 2, chip #'s 3 and 4, and chip #'s 5-8 for multi-site testing. Assume that each additional chip requires 250 more pin circuits. Will multi-site testing lower testing costs when the chip volume is 10 million per year? If so, by how much per year for the cases of 2, 4, and 8 chips using multi-site testing? Remember that you do not need more pin drivers for power supply and input signals to digital circuits when you switch to multi-site testing.