

Spring 2008
TESTING OF
ULTRA LARGE SCALE INTEGRATED CIRCUITS
16:332:576
Homework 3
REQUIRED

Assigned Feb. 8, 2008 – Due Feb. 29, 2008

Reading Assignment: Chapter 5

1 Logic and Fault Simulation

Write a true-value fault simulation program for combinational logic. Represent signals by two-state (0, 1) logic. The inputs to the program are: (1) an input vector file, (2) a flat circuit description in the Rutmod format, (3) a user-supplied list of signals (default primary outputs) for which simulated values are desired, and (4) a list of faults to be simulated. Each fault should be on a single line of a file in the format: *from signal #, to signal #* (the gate that the signal fans into), and *stuck-at value* (0 or 1). If the signal is not a fanout stem, *to signal #* should be 0. The output of the program should be a table of signal values. Use your program to verify the operation of a four-bit ripple-carry adder using the vectors of Table 5.1 in the textbook. Execute the following steps:

1. Manually compute the output of each vector
2. Run the fault simulator to verify that your circuit produces correct outputs.
3. Run the fault simulator for these faults:

C_0 sa0
 C_0 sa1
 A_1 sa0
 B_3 sa1

Your fault simulator must report which vector each fault was detected on, and it must report the difference in the primary outputs caused by the fault.

Prepare a report (no longer than 5 pages) on the program (algorithm, user manual), and the results of (a), (b), and (c). The program listing should be attached and can be in addition to the 5 pages.

If you do not do this homework, you will have an additional mandatory homework of writing a PODEM automatic test-pattern generator.