Spring 2008
TESTING OF
ULTRA LARGE SCALE INTEGRATED CIRCUITS
16:332:576
Homework 6
Assigned Feb. 29, 2008 – Due March 14, 2008

Reading Assignment: Chapter 8

1 Sequential Automatic Test Pattern Generation

8.21 *Pseudo-combinational circuit.* Derive a combinational circuit by replacing all flip-flops with shorting wires in the circuit of Figure 1. This is called the *pseudo-combinational transformation*. Generate a test for the fault d sa1 in the transformed circuit. Verify that the vector sequence obtained by repeatedly applying this vector four times will detect the d sa1 fault in the original sequential circuit. Note that the number of repetitions equals the *sequential depth* + 1.

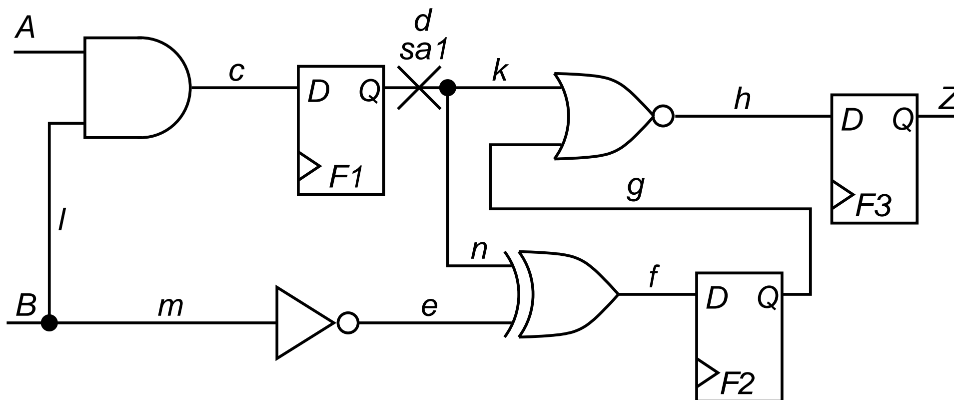

Figure 1: Circuit for Problem 8.21.

8.22 *Sequential ATPG.* Using *drivability measures* and *reverse time processing*, generate a test for the fault ac sa0 in the circuit of Figure 2.

8.23 *CONTEST.* Generate a test for the faults s sa0, t sa0, and v sa1 in the circuit in Figure 2 using the CONTEST algorithm. Use this random vector initialization sequence:

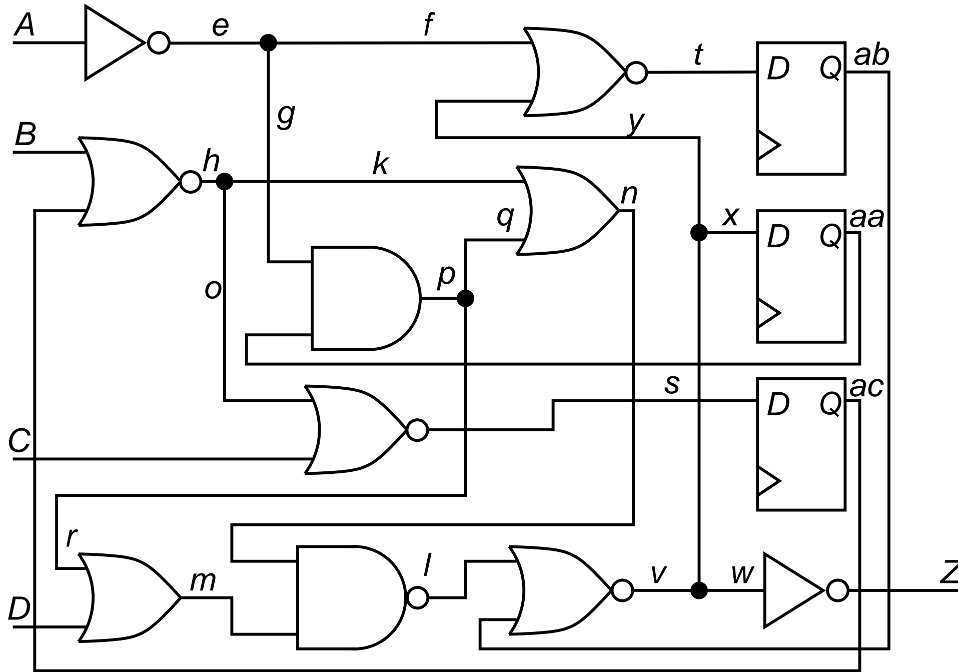

Figure 2: Circuit for Problems 8.22, 8.23, and 8.26 [1].

$$1001 \Rightarrow 0100 \Rightarrow 1110 \Rightarrow 0110 \Rightarrow 0000 \Rightarrow 0001$$

For CONTEST Phases 2 and 3, use the Unit Hamming Distance heuristic to generate additional trial vectors. In Phase 3, if the test generator gets trapped in a local cost minimum, abort ATPG for the fault.

8.24 *Oscillation fault.* The synchronous in Figure 3 is designed to have no memory state. Derive a test for the fault d sa0 and show that this is an *oscillation fault.* Redesign the fault-free function as a purely combinational circuit.

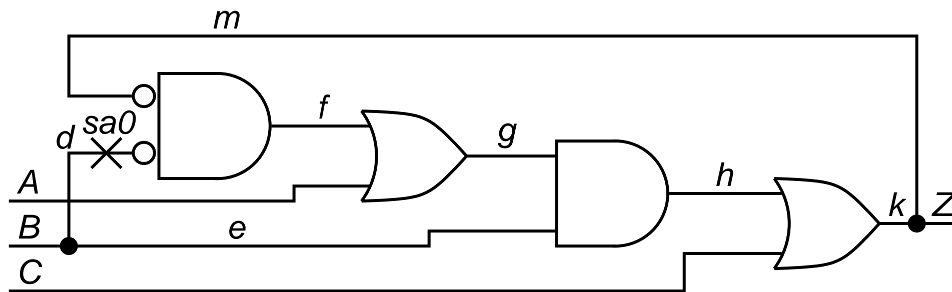

Figure 3: Circuit for Problem 8.24.

8.25 *Potentially-detectable fault.* Derive a test for the *potentially-detectable fault* CLK sa0 in the circuit of Figure 4. Also, derive a test for B sa1 and classify the type of this fault.

8.26 *Sequential ATPG.* Derive a test for the fault t sa0 in the circuit of Figure 2 using a sequential version of PODEM. Start at the time frame after the time frame of fault activation (frame 0), and propagate the fault to a PO in that time frame. Then, visit the immediately previous

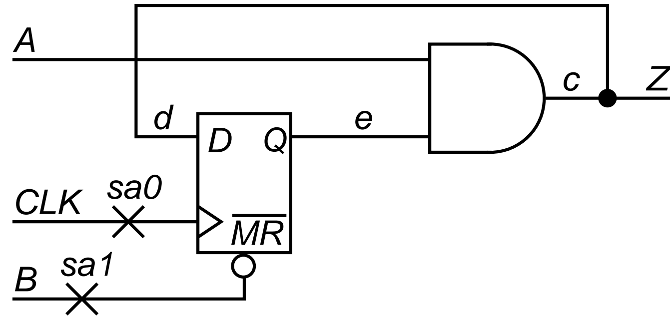

Figure 4: Circuit for Problem 8.25.

time frame (frame -1) and activate the fault, while justifying the present state for time frame 0. Notice how much easier this is than using CONTEST to detect the fault.

References

[1] F. Brglez, D. Bryan, and K. Kozminski. Combinational Profiles of Sequential Benchmark Circuits. In *Proc. of the International Symp. on Circuits and Systems*, pages 1929–1934, May 1989.