

14:332:438 Capstone Design – Computer Systems, VLSI Track
Spring 2008
Electrical and Computer Engineering Department
School of Engineering
Rutgers University

January 24, 2008

PHILOSOPHY:

This is the design companion course to 14:332:479 *Introduction to VLSI Design*. This is exclusively a project design course, and your entire grade is determined by your group project. You will apply the concepts you learned in 332:479 in order to design a large hardware system in this course, as a single chip. The entire class will be organized into 6-person design teams, each of which will complete a significant project by the end of the term. Part of your course grade is determined by the success of your project team, and the rest of your grade is determined by the quality of your own design effort.

We will design and make individual chip designs in this course using commercial VLSI Design software donated by Cadence and Synopsys Corporations. You will be taught how to effectively use this software, which is used world-wide in the electronics industry.

COURSE DESCRIPTION:

Undergraduates in this course will first complete a chip layout for a short design project, which will be fabricated on the AMIS 0.6 micron fab. line. Then, they will organize into teams, and each team will design a significantly sized System-on-a-Chip project for the Taiwan Semiconductor Manufacturing Company 0.18 micron fab. line. A weekly 1 hour meeting will be arranged for each team. There will be a meeting at the end of the course for final project presentations.

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Course Web Site:	http://www.caip.rutgers.edu/~bushnell
Office Hours:	Tuesday, Thursday 12:30-3:30 p.m.
Lecture Times:	Friday, 3:20 p.m. - 6:20 p.m. 1st Meeting 1/25/08
Classroom:	Eng. B-120
Course Laboratory:	Rooms CORE 601A and CORE 533
Lab Telephone:	(732) 445-6400 X 275

PREREQUISITES:

- 332:231 Digital Logic Design
- 332:252 Programming Methodology I
- 332:361 Electronic Devices
- 332:366 Digital Electronics
- 332:368 Digital Electronics Lab.
- 332:479 Introduction to VLSI Design

COREQUISITES:

- 332:331 Computer Architecture and Assembly Language
- 332:333 Computer Architecture Laboratory

VERY HELPFUL COURSES:

- 332:361 Electronic Devices
- 332:362 Analog Electronics
- 332:465 Physical Electronics

TWO-TERM SEQUENCE: This required course is the second part of a two-term sequence. This course is a pure design course, with little academic content, and the combination of the 332:479 and 332:438 courses satisfies the ECE Dept. capstone design course requirement.

TEXTS:

- Neil Weste and David Harris, *CMOS VLSI Design: A Systems Perspective*, third edition. Reading, MA: Addison-Wesley, 2005, ISBN # 0-321-14901-7.
- Michael L. Bushnell and Vishwani D. Agrawal, *Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits*, third printing. Boston: Kluwer Academic Publishers, 2000 (optional), ISBN #0-7923-7991-8.

Some material will be covered only in lecture. The textbooks are available now at the Rutgers University Bookstore.

LABORATORY:

- You should obtain Cartesian graph paper and a set of colored pencils (red, yellow, green, blue, black, purple) for drawing *sticks* diagrams.
- Arrangements for laboratory access will be announced later.
- A subsequent memo will describe the laboratory regulations.
- This course is always under development, and its content is subject to change. Constructive suggestions from students are greatly appreciated.

ASSUMED BACKGROUND:

- Elementary Transistor Electronics
- Boolean Algebra
- MOS Digital Logic Design – combinational and sequential circuits, SSI & MSI
- SR, D, T, and JK Flip-Flops and SR and D Latches
- Number Systems (Bases 2, 8, and 16) and Coding systems
- Signed Magnitude, Ones-complement, and Twos-complement representations
- Register Transfer Level Design
- Elementary Diode and Transistor Theory
- Elementary Microprogramming
- Interrupt Systems
- Microprocessors and Minicomputers
- Electrical Network Theory
- Introductory VLSI Design

If you are unfamiliar with any of these concepts, you should drop this course.

GRADING:

Tiny Chip Project	20%
Large Project	80%
Total	100%

POLICIES:

1. STUDENTS ARE EXPECTED TO COLLABORATE ON THE LARGE PROJECT, WHICH MUST BE A GROUP EFFORT OF AT LEAST 5 STUDENTS.
2. The schedule below indicates when each component of the project is due. The penalty for missing a due date is that you lose 1/2 of a letter grade in this course. The only exceptions will be in the case of illness, death in the family, extraordinary family circumstances, or computer failure at Rutgers.
3. All course materials are available on the course web site:
<http://www.caip.rutgers.edu/~bushnell>
4. Do your lab work early – this will give you a chance to get on the computer. Most students let lab work wait until the night before it is due, and then are unable to get a computer because they are all taken.

GRADING PROCEDURE:

The course grading is intended to encourage you to use a structured design methodology, in order to accelerate your design activities. All layouts and circuits will be graded according to this procedure:

1. If there is no logic schematic from the Cadence System, the grade is 0.
2. If there are no convincing logic simulation results from the Cadence System, the grade is 0.
3. For every redundant logic signal in the circuit, you lose 2 points. The Rutgers Automatic Test-Pattern Generators **EST** and **spectralATPG** will find these redundant logic gates in your circuit automatically. You are **REQUIRED** to supply the **EST/spectralATPG** commentary for each of your logic designs to show that there is no redundant logic.
4. If you do not list the logic level circuit test-patterns, the grade is 0.
5. For all layouts, we will subtract 2 points for every logic error and 1 point for every physical design rule error. Then, we will multiply the remaining score by the ratio of the solution layout area to your layout area. The net effect is that layouts with logic and design rule errors or that use excessive chip area are severely penalized. Hand drawn layouts (with colored pencils on paper) will get a grade of 0.
6. If you do not provide analog simulation results for the circuit extracted from the layout, the grade is 0.

The purpose of this grading procedure is not to harass you or embarrass you, but to save you **ENORMOUS** amounts of time during your chip design. It is now routine in the semiconductor industry for a designer to rapidly produce a 10 million transistor chip using CAD tools and following the structured design methodology taught in this course.

COURSE MEETING OUTLINE:

#	Description	Date
1	PROJECT TEAM ORGANIZATION	1/24/08
2-27	WEEKLY PROJECT TEAM MEETINGS	2/1/08 – 4/25/08
28	FINAL PROJECT PRESENTATIONS	5/2/08

PROJECT SCHEDULE

Date	Required Activity Description	Late Penalty	Grade Effect
2/1/08	Project Proposals with Work Assignment Due	- 1/2 Course Grade	A
2/8/08	Project Specification & System Block Diagram	- 1/2 Course Grade	A-
2/15/08	System Timing Diagram Due	- 1/2 Course Grade	B+
2/22/08	Economic and Cost Analysis of Project Due	- 1/2 Course Grade	B
2/22/08	Chip Power Estimation Due	- 1/2 Course Grade	B-
2/29/08	Behavioral VERILOG Code Due	- 1/2 Course Grade	C+
2/29/08	Behavioral VERILOG Simulation Due	- 1/2 Course Grade	C
3/14/08	Synthesized VERILOG Logic Due	- 1/2 Course Grade	C-
3/14/08	Logic VERILOG Simulation Due	- 1/2 Course Grade	D+
3/14/08	Chip Slice Plan Due	- 1/2 Course Grade	D
3/14/08	Chip Floor Plan Due	- 1/2 Course Grade	D-
3/21/08	Testing Method Hardware Due	- 1/2 Course Grade	F+
4/18/08	Leaf Cell Layout Library Due	- 1/2 Course Grade	F
4/18/08	Tiny Chip Project Due	- 1/2 Course Grade	F-
4/25/08	Testing Fault Coverage and Test Patterns Due	- 1/2 Course Grade	F- -
4/25/08	Complete Routed Chip Layout with Pads Due	- 1/2 Course Grade	F- -
4/25/08	Project Safety and Environmental Impact Statement Due	- 1/2 Course Grade	F- -
4/25/08	Routed Chip Timing Analysis Due	- 1/2 Course Grade	F- -
5/2/08	Final Project Presentation Due	- 1/2 Course Grade	F- -
5/2/08	Final Project Report Due	- 1/2 Course Grade	F- -

Your final projects will be graded on the following criteria:

- Quality of the Project Specifications.
- Logical correctness (shift registers that don't shift will cost you points).
- Speed and throughput (hardware that cannot achieve your specified clock rate will cost you points).
- Correct physical design.
- Correct use of logic and analog circuit simulation tools.
- Presence of a viable testing procedure for the hardware.
- Quality of the documentation (if it is a mess, you will lose points).
- Presence of a Cost Analysis for this Design.
- Presence of Environmental Impact and Health and Safety Description for this Design.

Verify logical correctness as you progress in the design phase, not after the whole thing is completed.

PROJECT IDEAS

Below are some project ideas. You need not choose a project from this list. It is not necessary that your project be a brand new innovation. However, I strongly encourage you to be creative. I will not accept any digital alarm clock or parallel multiplier designs. This course presents an exciting design opportunity, and each group must come up with its own project proposal! I hope

that your project will reflect some of the things I have been stressing in this course sequence, such as regularity, logical correctness, fault-tolerance, testing, high-speed arithmetic, etc.

1. Design a 64-bit microprocessor.
2. Design a 16-bit Digital Signal Processor.
3. Design a hierarchical memory system, with high-speed cache, DRAM, and flash DRAM implemented as a multi-level, virtual memory system.
4. Design a high-speed floating point arithmetic processor.
5. Design a programmable I/O controller.
6. Design an image processing hardware system that can do the Hough transform, the Discrete Cosine Transform, and all of the frequently-used transforms for image processing.
7. Design an advanced home automation and security system.
8. Design a map routing system for an automobile.
9. Design a knock-out switch for an Asynchronous Transfer Mode (ATM) internet switch.
10. Design a baseband processor and a microprocessor for one of the communication system protocols of our time: GPS, 802.11, 802.16, Bluetooth, CDMA Cellular Telephone, etc.
11. Design an MPEG player.
12. Design a Personal Data Assistant.

These are only suggestions, but represent some of the better hardware designs that have been done at Carnegie Mellon, Duke, and Rutgers.

REFERENCE BOOKS:

- H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI*, Reading, MA: Addison-Wesley, 1990, ISBN # 0-201-06008-6.
- M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory, & Logic VLSI Circuits*, 1st Edition. Boston: Kluwer Academic Publishers, 2000, ISBN #0-7923-7991-8.
- *Cadence Design System Manuals* (on-line).
- S. A. Campbell, *The Science and Engineering of Microelectronic Fabrication*, New York: Oxford U. Press, 1996, ISBN # 0-19-510508-7.
- T. Dillinger, *VLSI Engineering*. Englewood Cliffs, NJ: Prentice Hall, 1988, ISBN # 0-13-942731-7 025.
- J. E. Franca and Y. Tsividis, *Design Analog-Digital VLSI Circuits for Telecommunications and Signal Processing*, Englewood Cliffs, NJ: Prentice-Hall, 1994, 2nd Edition, ISBN # 0-13-203639-8.
- S. Ghandhi, *VLSI Fabrication Principles. Silicon and Gallium Arsenide*, 2nd Edition, New York: John Wiley & Sons, 1994, ISBN # 0-471-86833-7.

- C. Hu, editor, *Nonvolatile Semiconductor Memories, Technologies, Design, and Applications*. Piscataway, NJ: IEEE Press, 1991, ISBN # 0-87942-269-6.
- S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits Analysis and Design*. New York: McGraw-Hill, 1996, ISBN # 0-07-038046-5.
- Tracy Kidder, *The Soul of a New Machine*. Boston: Little, Brown and Co., 1981, ISBN # 0-316-49170-5. This book won the Pulitzer Prize.
- K. Lee, M. Shur, T. A. Fjeldly, and T. Ytterdal, *Semiconductor Device Modeling for VLSI*, Englewood Cliffs, NJ: Prentice-Hall, 1993, ISBN # 0-13-805656-0.
- B. Leung, *VLSI for Wireless Communication*, Upper Saddle River, NJ: Prentice-Hall, 2002, ISBN # 0-13-861998-0.
- C. Mead, *Analog VLSI and Neural Systems*, ISBN # 0-201-05992-4.
- J. Milman and C. Halkias, *Integrated Electronics, Analog and Digital Circuits and Systems*, New York: McGraw-Hill Book Co., 1992, ISBN # 0-074-62245-5.
- Muroga, *Logic Design & Switching Theory*, Krieger Publishing Co., ISBN # 1-57524-036-X.
- J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits A Design Perspective*, 2nd edition, Upper Saddle River: NJ, Pearson Education, Inc., 2003, ISBN #0-13-597444-5.
- K. Roy and S. C. Prasad, *Low-Power CMOS VLSI Circuit Design*, New York: John Wiley & Sons, 2000, ISBN #0-471-11488-X.
- Masakazu Shoji, *CMOS Digital Circuit Technology*. Englewood Cliffs, NJ: Prentice Hall, 1988, ISBN # 0-13-138850-9.
- Michael John Sebastian Smith, *Application-Specific Integrated Circuits*. Reading, MA: Addison Wesley Longman, Inc., 1997, ISBN # 0-201-73357-9.
- S. M. Sze, *VLSI Technology*, second edition. New York: McGraw-Hill Book Co., 1988, 2nd Edition, ISBN # 0-07-062735-5.
- D. Thomas and P. Moorby, *The Verilog Hardware Description Language*, Boston: Kluwer Academic Publishers, 5th Edition, 2003, ISBN # 1-4020-7089-6.
- R. R. Troutman, *Latchup in CMOS Technology, The Problem and Its Cure*. Boston: Boston: Kluwer Academic Publishers, 1986, ISBN # 0-89838-215-7.
- J. P. Uyemura, *CMOS Logic Circuit Design*, Boston: Kluwer Academic Publishers, 1999, ISBN # 0-7923-8452-0.
- J. P. Uyemura, *Introduction to VLSI Circuits and Systems*, New York: John Wiley & Sons, 2002, ISBN # 0-471-12704-3.
- John F. Wakerley, *Digital Design Principles and Practices*, Prentice Hall.
- W. Wolf, *Modern VLSI Design System-on-Chip Design*, Upper Saddle River, NJ: Prentice-Hall, 2002, 3rd Edition, ISBN # 0-13-061970-1.
- K.-S. Yeo, S. S. Rofail, and W.-L. Goh, *CMOS/BiCMOS ULSI Low Voltage, Low Power*, Upper Saddle River, NJ: Prentice-Hall, 2002, ISBN # 0-13-032162-1.